

Technical drawing of a U-shaped component. The dimensions are as follows:

- Width: 1.00mm (+/- 0.10mm)
- Height: 3.80mm (+/- 0.10mm)
- Top Radius: 0.50mm (+/- 0.10mm)

Detail 1

Technical drawing of a U-shaped part with the following dimensions:

- Top horizontal edge: 1.00mm ($\pm 0.10\text{mm}$)
- Right vertical edge: 2.00mm ($\pm 0.10\text{mm}$)
- Bottom horizontal edge: 2.00mm ($\pm 0.10\text{mm}$)

Detail 2

Technical drawing of a semi-circular profile. The drawing shows a semi-circle with a horizontal diameter and a vertical radius. The dimensions are indicated as follows:

- Horizontal dimension (Diameter): 2.00mm ($\pm 0.10\text{mm}$)
- Vertical dimension (Radius): 4.00mm ($\pm 0.10\text{mm}$)

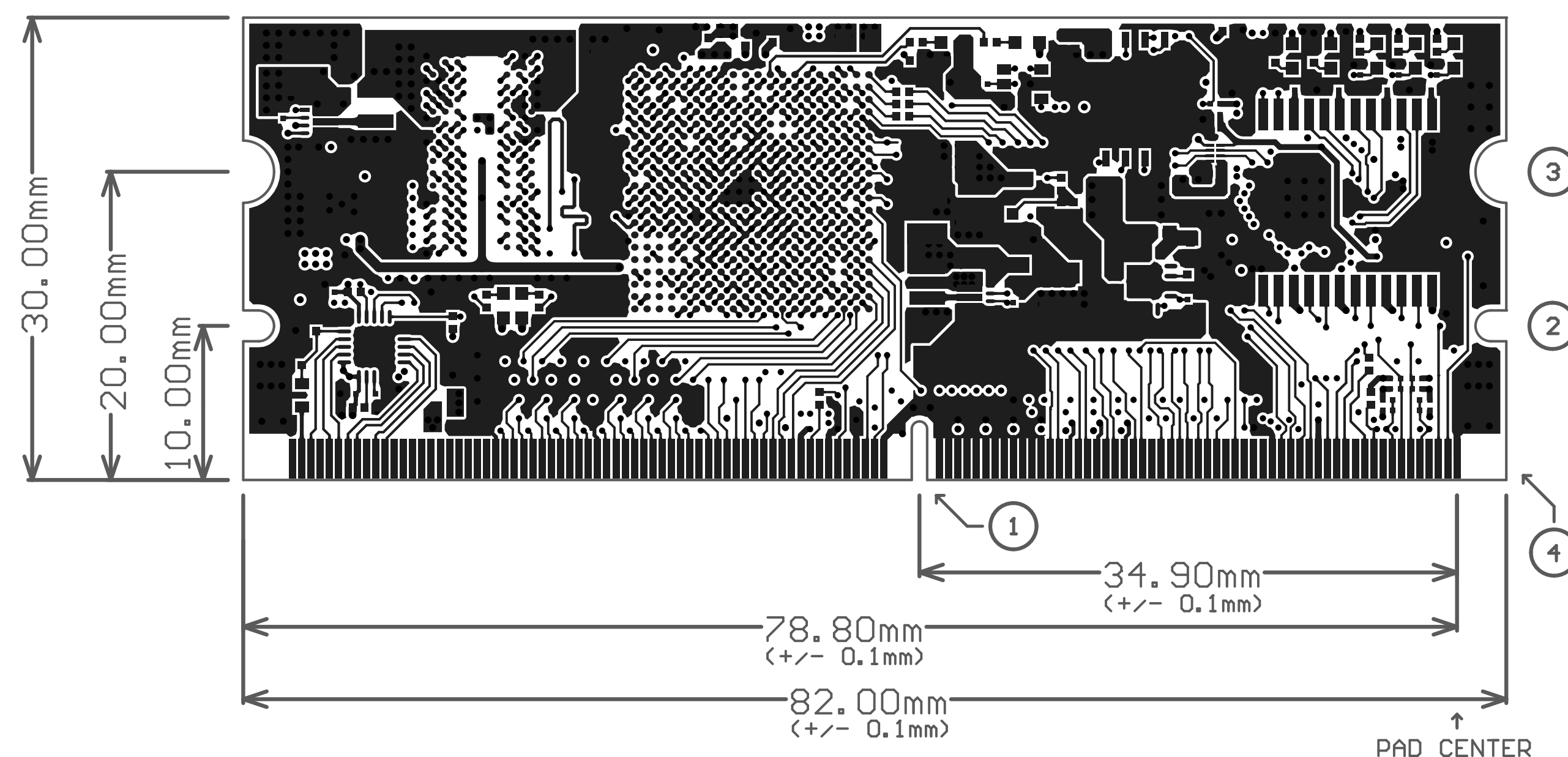
Detail 3

Technical drawing of a 10mm diameter hole in a 10mm thick plate. The hole has a 0.15mm chamfer. Dimensions are given with tolerances: 1.00mm (hole diameter), 0.15mm (chamfer height), and 10mm (plate thickness).

Detail 4

(PCB side view)

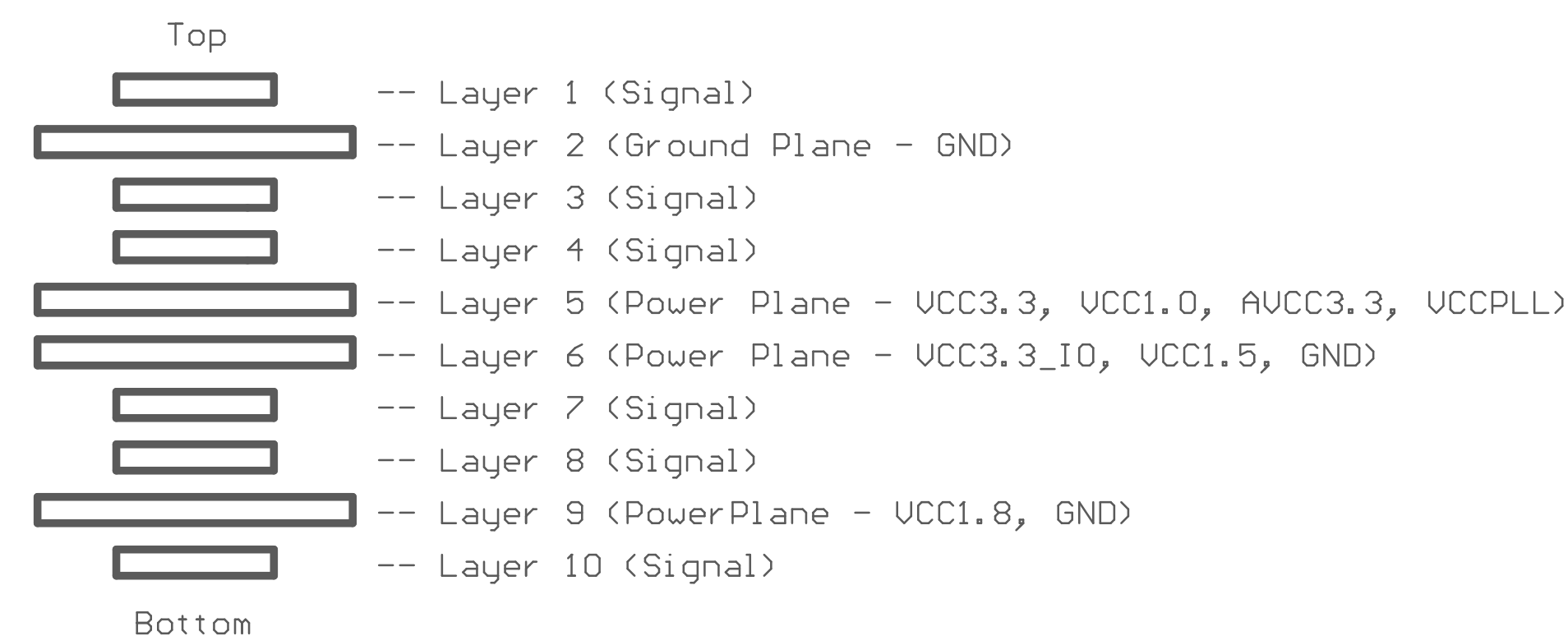
UW-IPMC MEZZANINE (revB)
Layer 1 - Signal (Copper)



Specifications:

1. Dielectric material is Tetrafunctional FR-4 with Tg > 170 C
2. Overall thickness is 1.0mm +/- 0.10mm
3. Board dimensions are 82 by 30mm with tolerances of +/- 0.15mm unless specified in drawing.
4. Panelization
 - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - b. Panels should contain fiducial marks for X,Y alignment
5. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
 40 Ohm: 6 mil tracks in artwork
 50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
 40 Ohm: 9.5 mil tracks in artwork
 50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
6. All layers use 1/2 oz. copper (before plating)
7. Holes:
 - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - d. Drills are plated-through holes and their locations are given in a separate drill file.
8. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface.
 Area to receive hard gold finish is identified in two separate photoplot layers.
 Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
9. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
10. Red colored solder mask shall be applied to both top and bottom surfaces.
 Mask shall be photoimageable, with maximum thickness of 3 mils
11. Layers 2, 5, 6 and 9 are power planes and are INVERTED
12. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
 DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing.
 Testing report to be enclosed with the quality control documentation shipped with the boards.
17. Locations in IPC-D-356A file are given in 2.4 English units
18. South edge-to-edge connector details:
 - a. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup



Univ. of Wisconsin—Madison
Madison, WI 53706

ENGINEER:
Vicente, M.

PCB DESIGNER:
Vicente, M.

DATE:
06JUN2019

FILE NAME:
ZYNQ_IPMC.PCBDOC

TITLE:
ZYNQ-IPMC

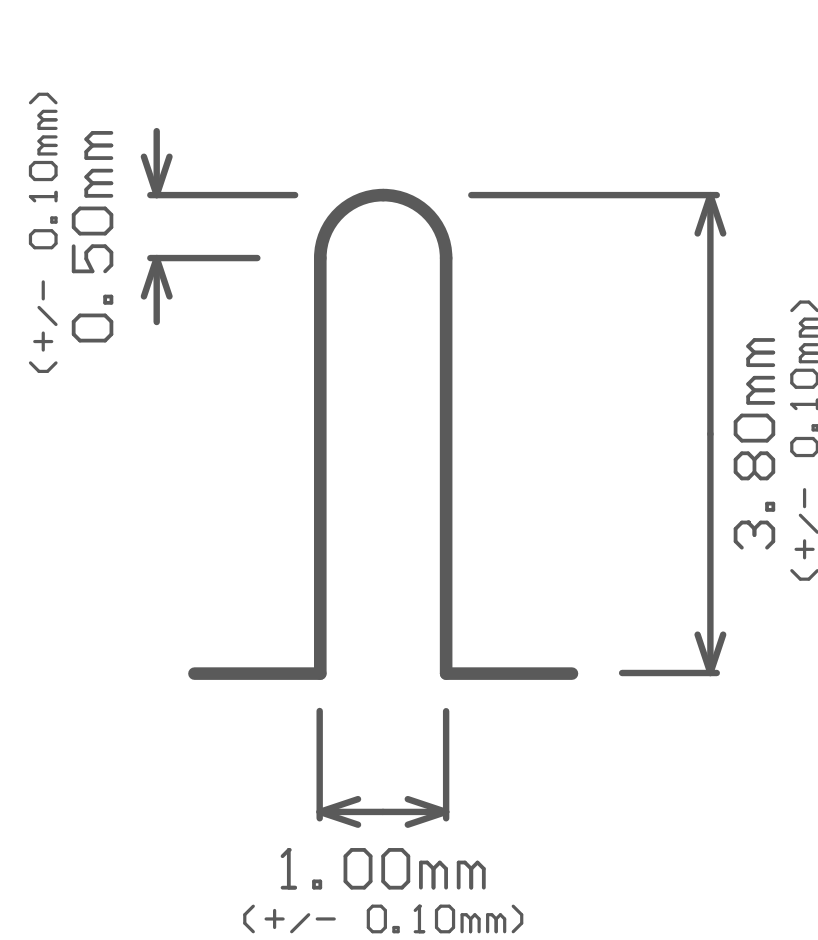
PART NO.:

REV:
revB1

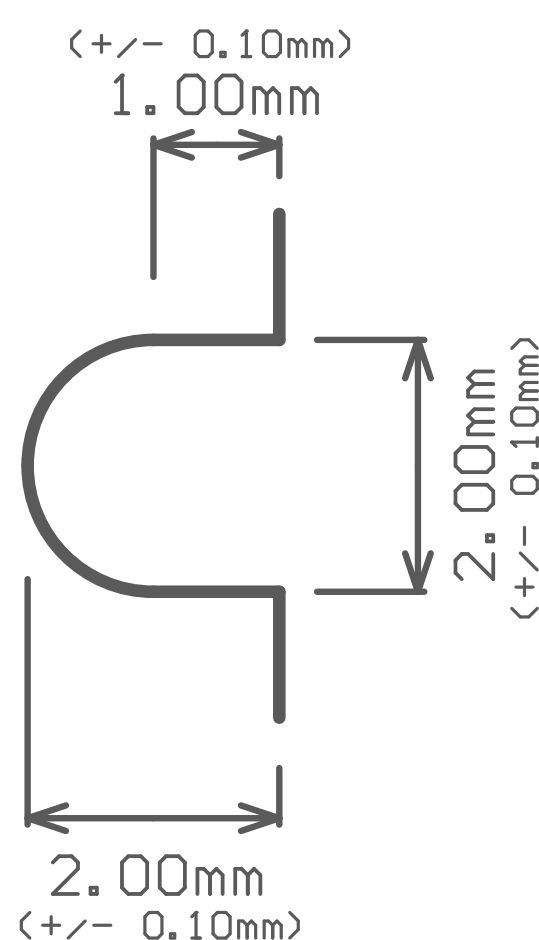
DWG NO:

SCALE:
1:1

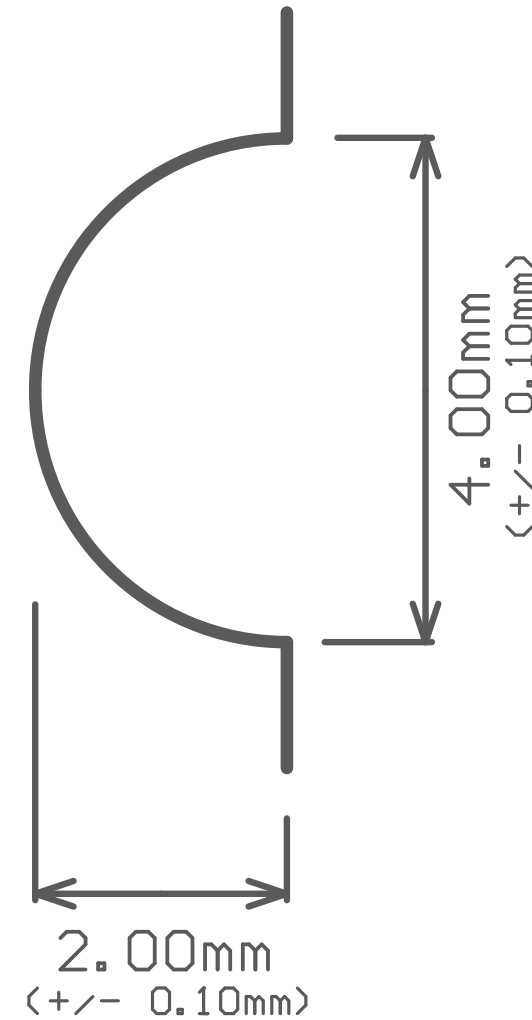
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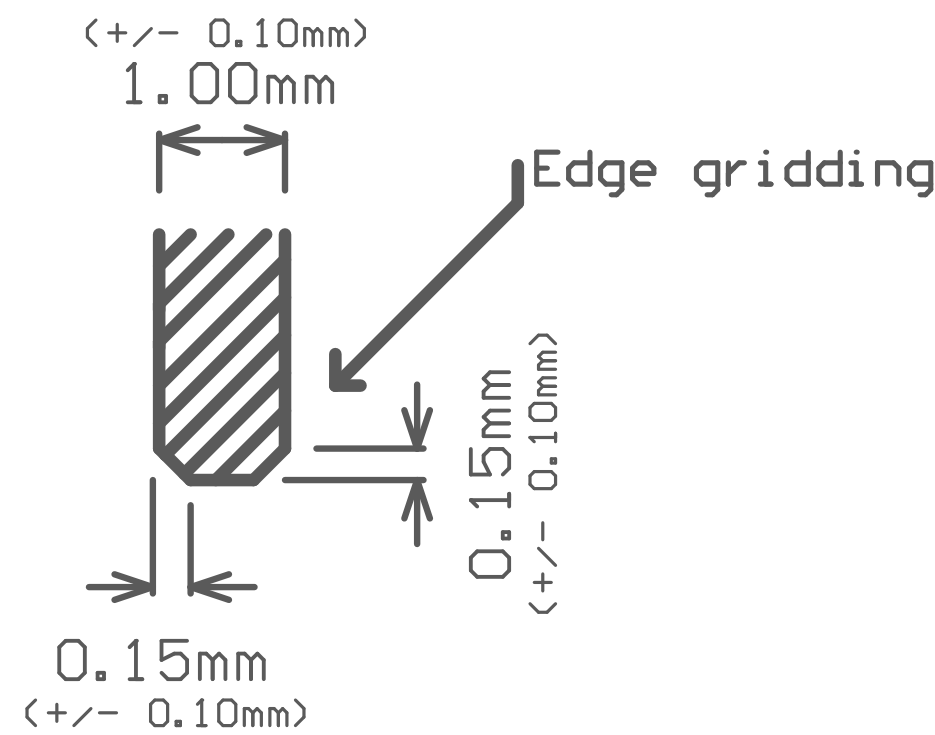
Detail 1



Detail 2



Detail 3

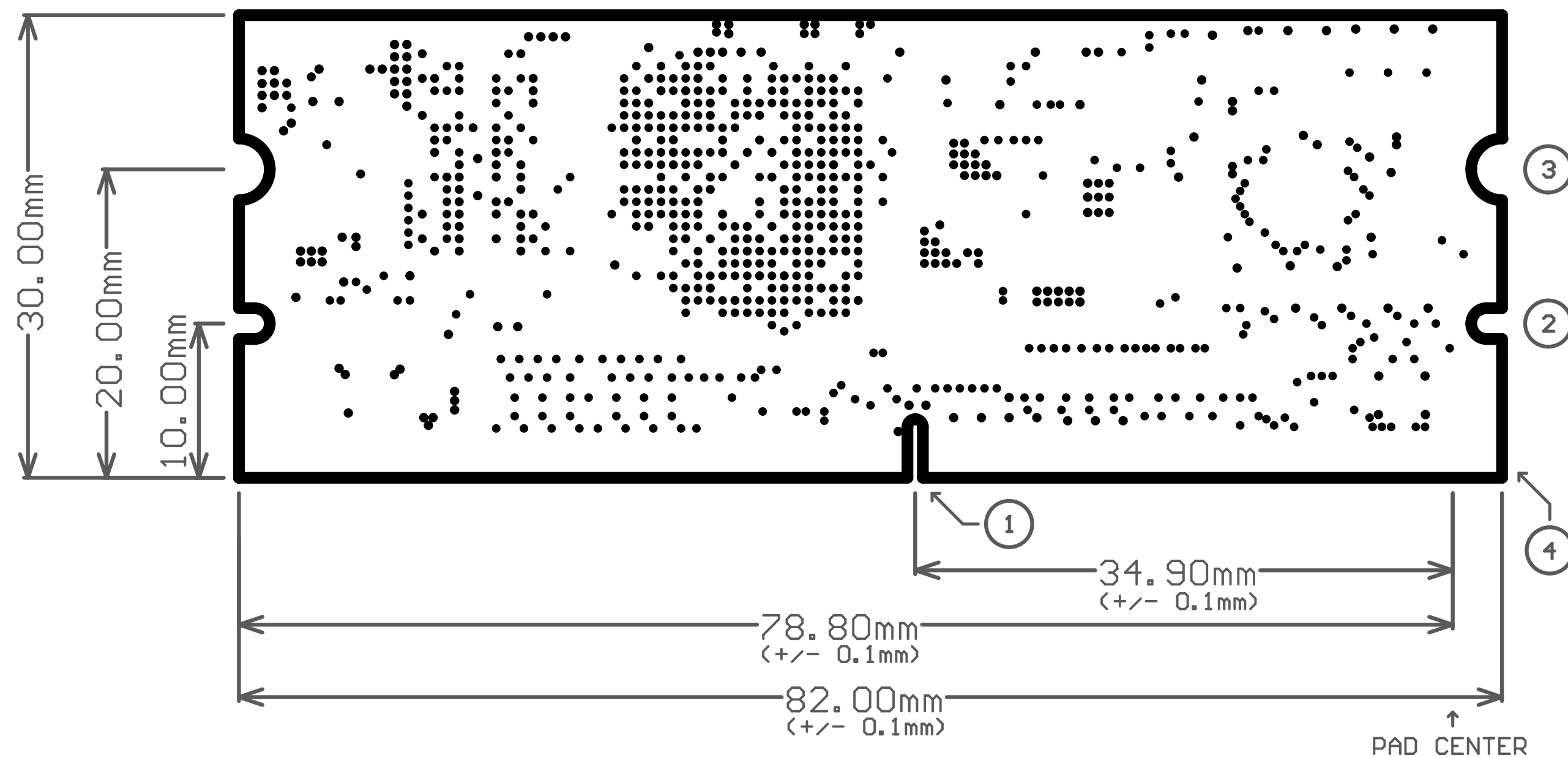


Detail 4
(PCB side view)

B

UW-IPMC MEZZANINE (revB)

Layer 2 - Ground Plane (Copper, Mask)



C

Specifications:

- Dielectric material is Tetrafunctional FR-4 with $T_g > 170\text{ }^{\circ}\text{C}$
- Overall thickness is 1.0mm $\pm 0.10\text{mm}$
- Board dimensions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
- Panelization
 - Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - Panels should contain fiducial marks for X,Y alignment
- Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
- All layers use 1/2 oz. copper (before plating)
- Holes:
 - Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - Drills are plated-through holes and their locations are given in a separate drill file.
- Finish:
 - Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - Overall board finish is immersion gold.
- Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
- Red colored solder mask shall be applied to both top and bottom surfaces.
Mask shall be photoimagable, with maximum thickness of 3 mils
- Layers 2, 5, 6 and 9 are power planes and are INVERTED
- Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
- Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
- Combination of bow and twist shall not exceed 10 mils/inch along any direction
- Design origin is at the bottom-left corner of the PCB
- Testing:
 - All layers to undergo optical inspection (machine-based) of all layers before lamination
 - Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
DC resistance shall be 10 ohms or less
 - Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
- Locations in IPC-D-356A file are given in 2.4 English units
- South edge-to-edge connector details:
 - Details present in page 2 of the Molex 87783-0301 datasheet (included).

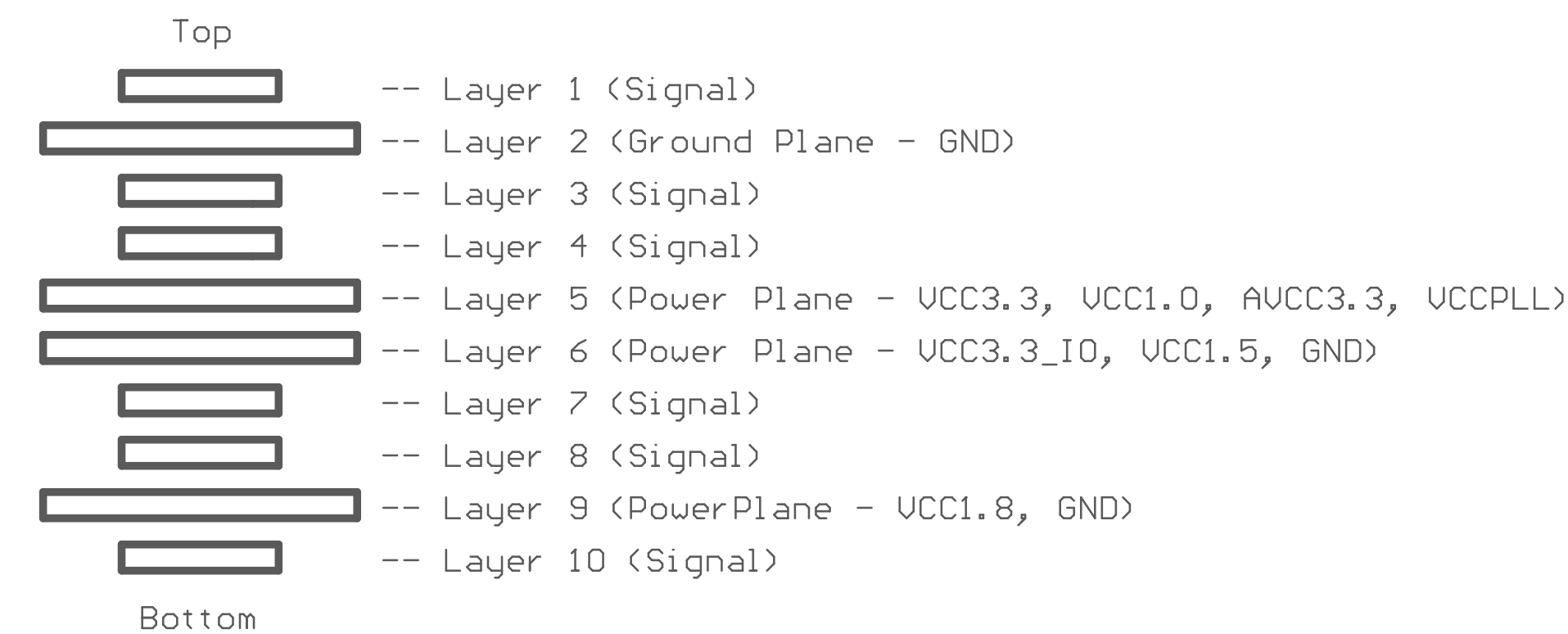
A

B

D

D

Layer Stackup



Univ. of Wisconsin—Madison Madison, WI 53706	ENGINEER: Vicente, M.	TITLE: ZYNQ—IPMC	
	PCB DESIGNER: Vicente, M.		
	DATE: 06JUN2019	PART NO.:	REV: revB1
	FILE NAME: ZYNQ_IPMC.PCBDOC	DWG NO:	SCALE: 1:1

A

B

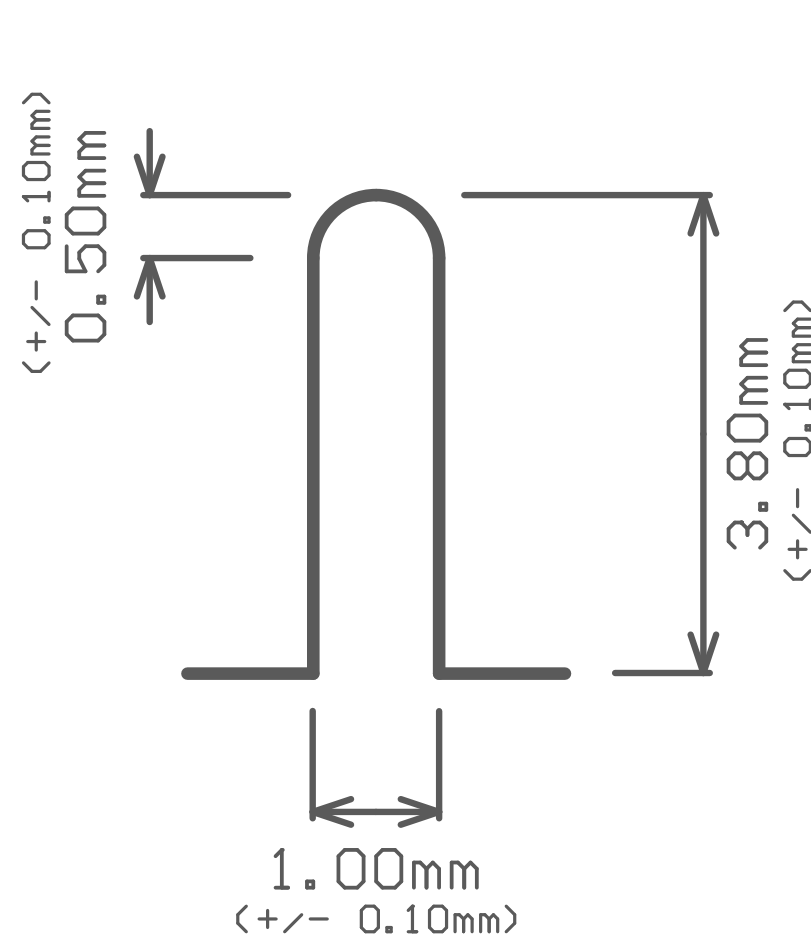
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D

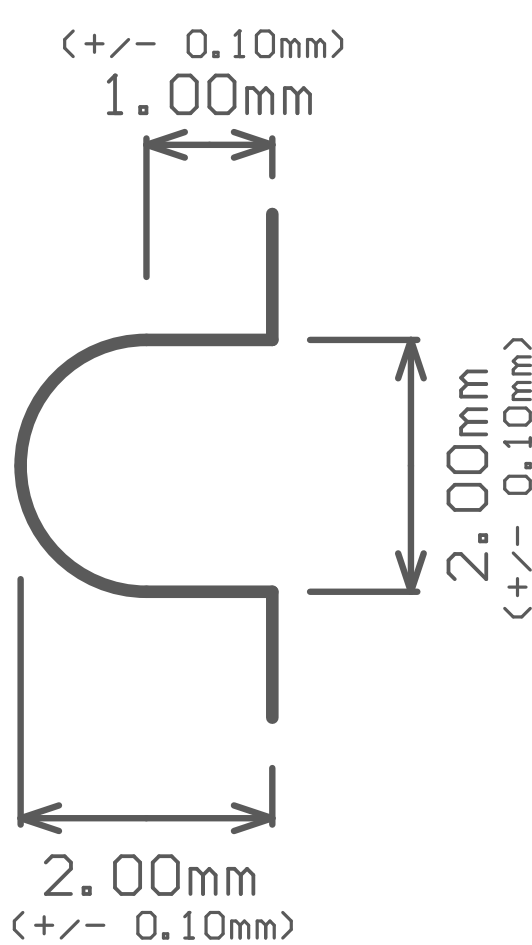
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B

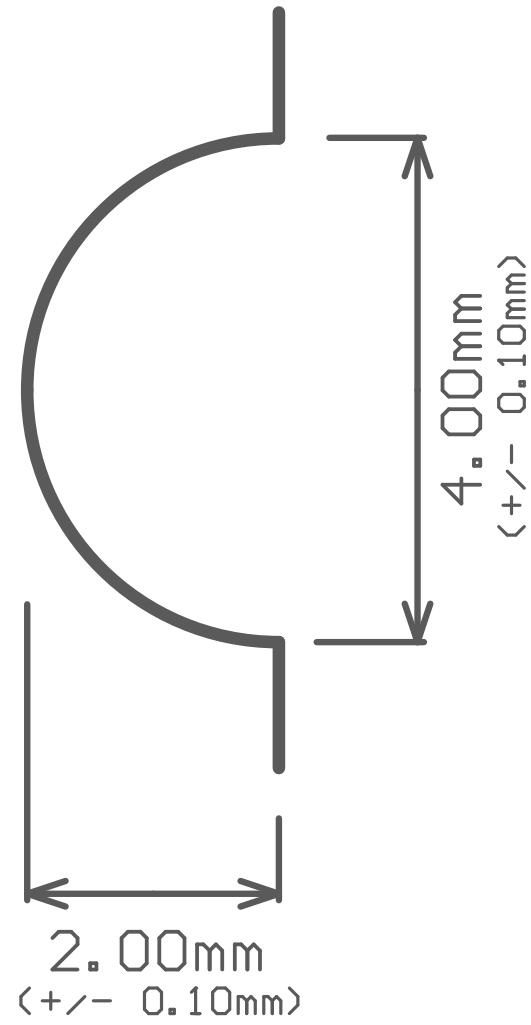
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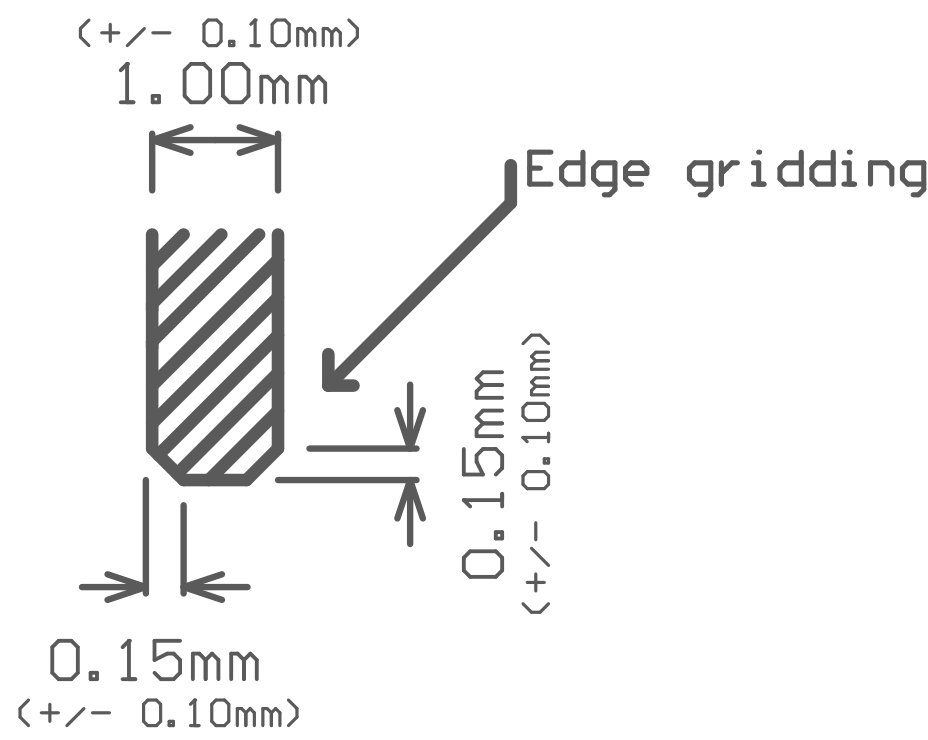
Detail 1



Detail 2



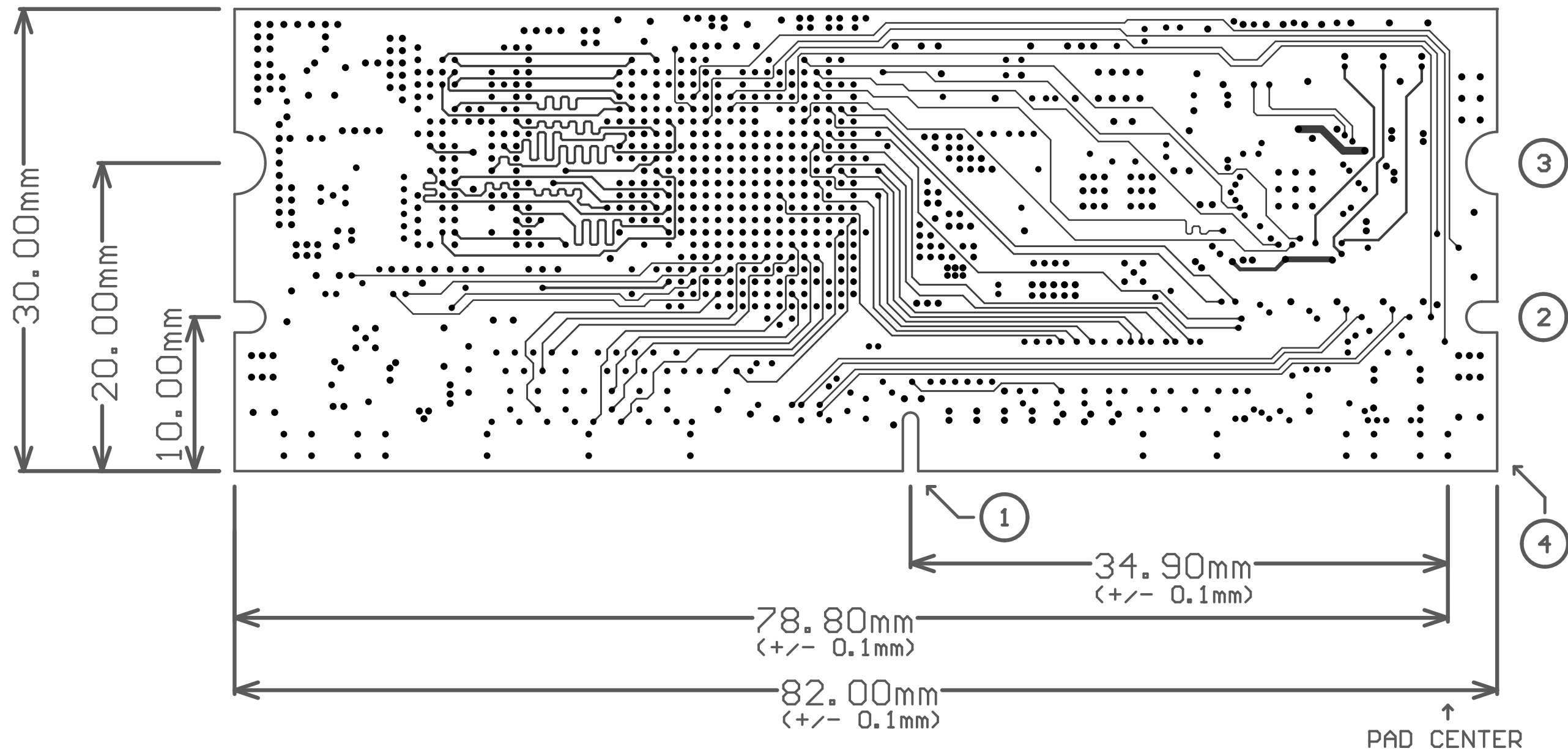
Detail 3



Detail 4
(PCB side view)

UW-IPMC MEZZANINE (revB)

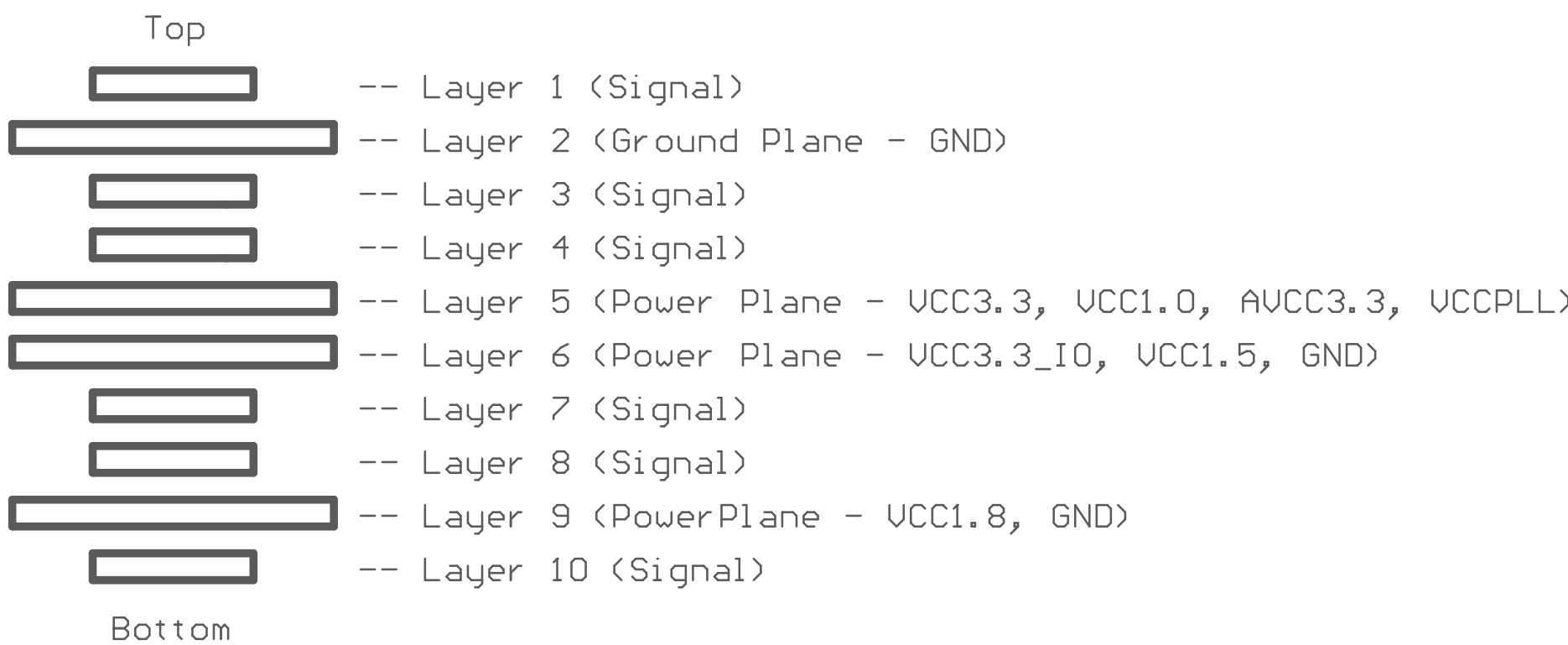
Layer 3 - Signal (Copper)



Specifications:

- Dielectric material is Tetrafunctional FR-4 with $T_g > 170^\circ\text{C}$
- Overall thickness is 1.0mm $\pm 0.10\text{mm}$
- Board dimensions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
- Panelization
 - Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - Panels should contain fiducial marks for X,Y alignment
- Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
- All layers use 1/2 oz. copper (before plating)
- Holes:
 - Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - Drills are plated-through holes and their locations are given in a separate drill file.
- Finish:
 - Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - Overall board finish is immersion gold.
- Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
- Red colored solder mask shall be applied to both top and bottom surfaces.
Mask shall be photoimageable, with maximum thickness of 3 mils
- Layers 2, 5, 6 and 9 are power planes and are INVERTED
- Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
- Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
- Combination of bow and twist shall not exceed 10 mils/inch along any direction
- Design origin is at the bottom-left corner of the PCB
- Testing:
 - All layers to undergo optical inspection (machine-based) of all layers before lamination
 - Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
- Locations in IPC-D-356A file are given in 2.4 English units
- South edge-to-edge connector details:
 - Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup



Univ. of Wisconsin—Madison
Madison, WI 53706

ENGINEER:
Vicente, M.

PCB DESIGNER:
Vicente, M.

DATE:
06JUN2019

FILE NAME:
ZYNQ_IPMC.PCBDOC

TITLE:
ZYNQ—IPMC

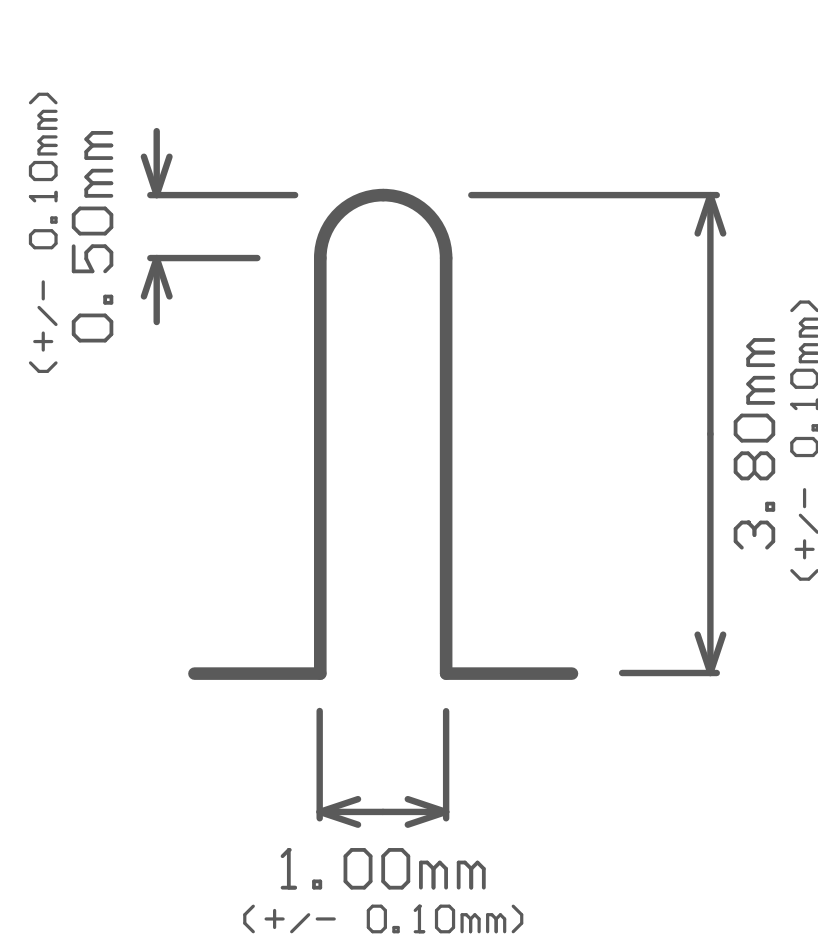
PART NO.:

DWG NO:

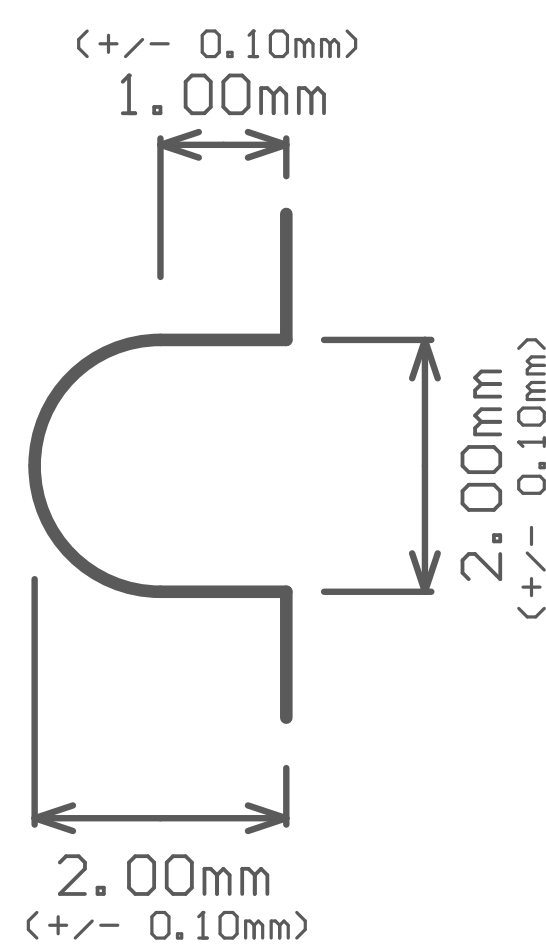
REV:
revB1

SCALE:
1:1

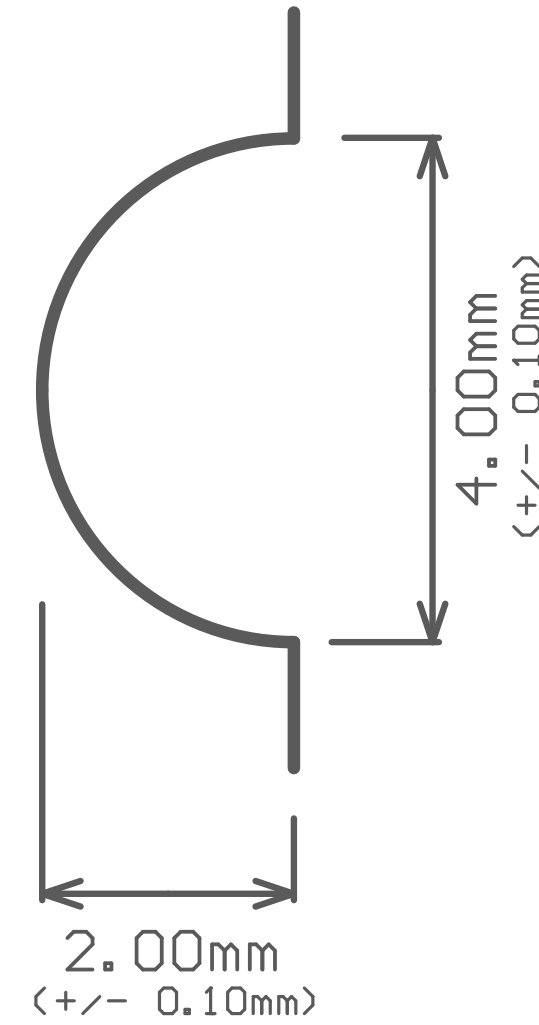
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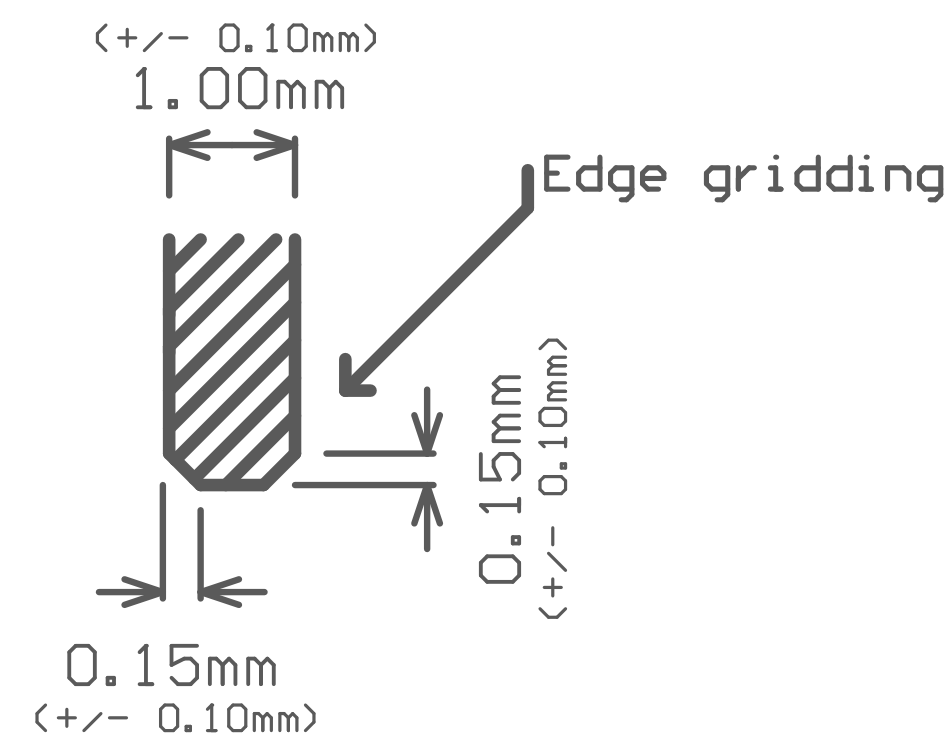
Detail 1



Detail 2



Detail 3

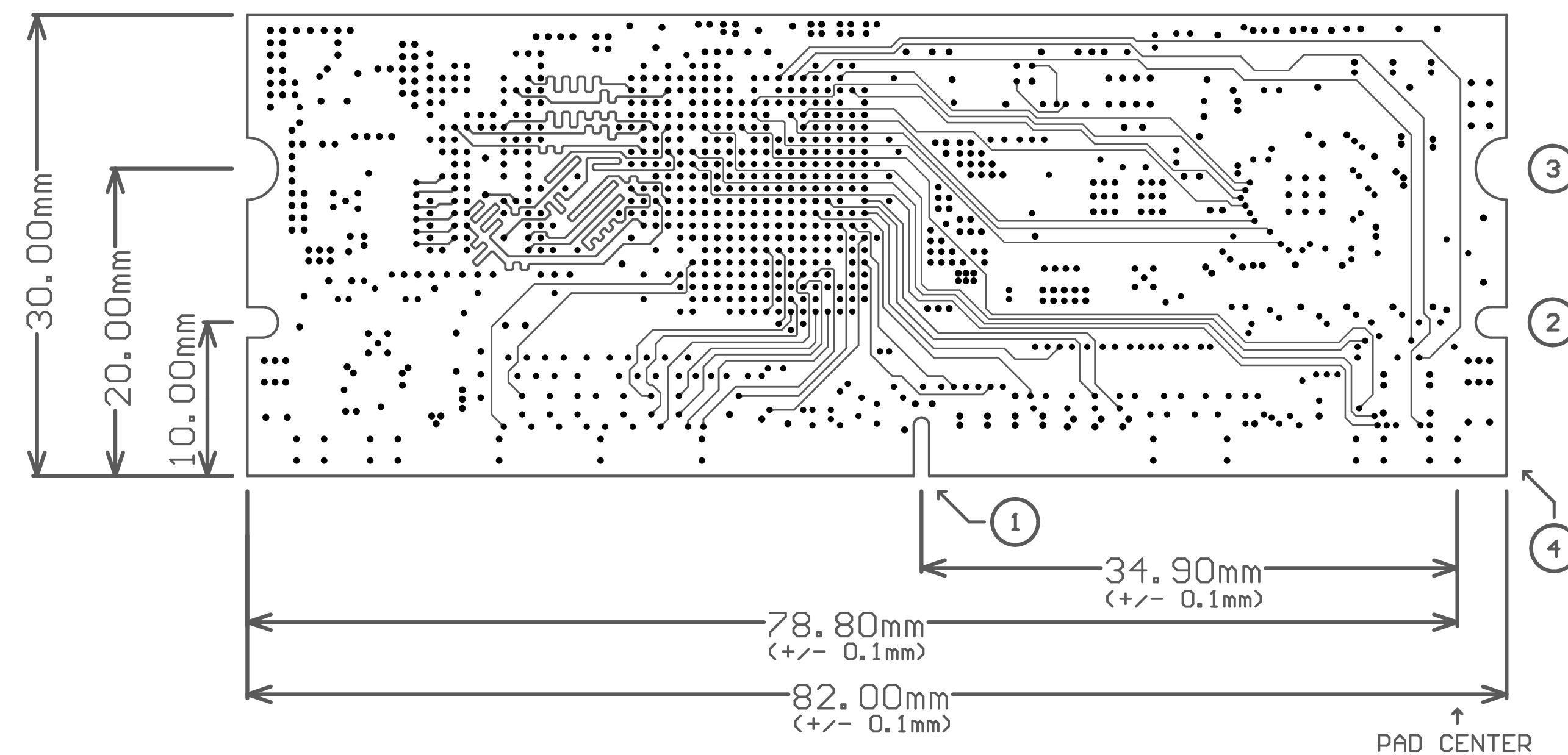


Detail 4
(PCB side view)

B

UW-IPMC MEZZANINE (revB)

Layer 4 - Signal (Copper)



C

Specifications:

- Dielectric material is Tetrafunctional FR-4 with $T_g > 170\text{ }^{\circ}\text{C}$
- Overall thickness is 1.0mm $\pm 0.10\text{mm}$
- Board dimentions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
- Panelization
 - Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - Panels should contain fiducial marks for X,Y alignment
- Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
- All layers use 1/2 oz. copper (before plating)
- Holes:
 - Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - Drills are plated-through holes and their locations are given in a separate drill file.
- Finish:
 - Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - Overall board finish is immersion gold.
- Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
- Red colored solder mask shall be applied to both top and bottom surfaces.
Mask shall be photomagable, with maximum thickness of 3 mils
- Layers 2, 5, 6 and 9 are power planes and are INVERTED
- Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
- Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
- Combination of bow and twist shall not exceed 10 mils/inch along any direction
- Design origin is at the bottom-left corner of the PCB
- Testing:
 - All layers to undergo optical inspection (machine-based) of all layers before lamination
 - Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
- Locations in IPC-D-356A file are given in 2.4 English units
- South edge-to-edge connector details:
 - Details present in page 2 of the Molex 87783-0301 datasheet (included).

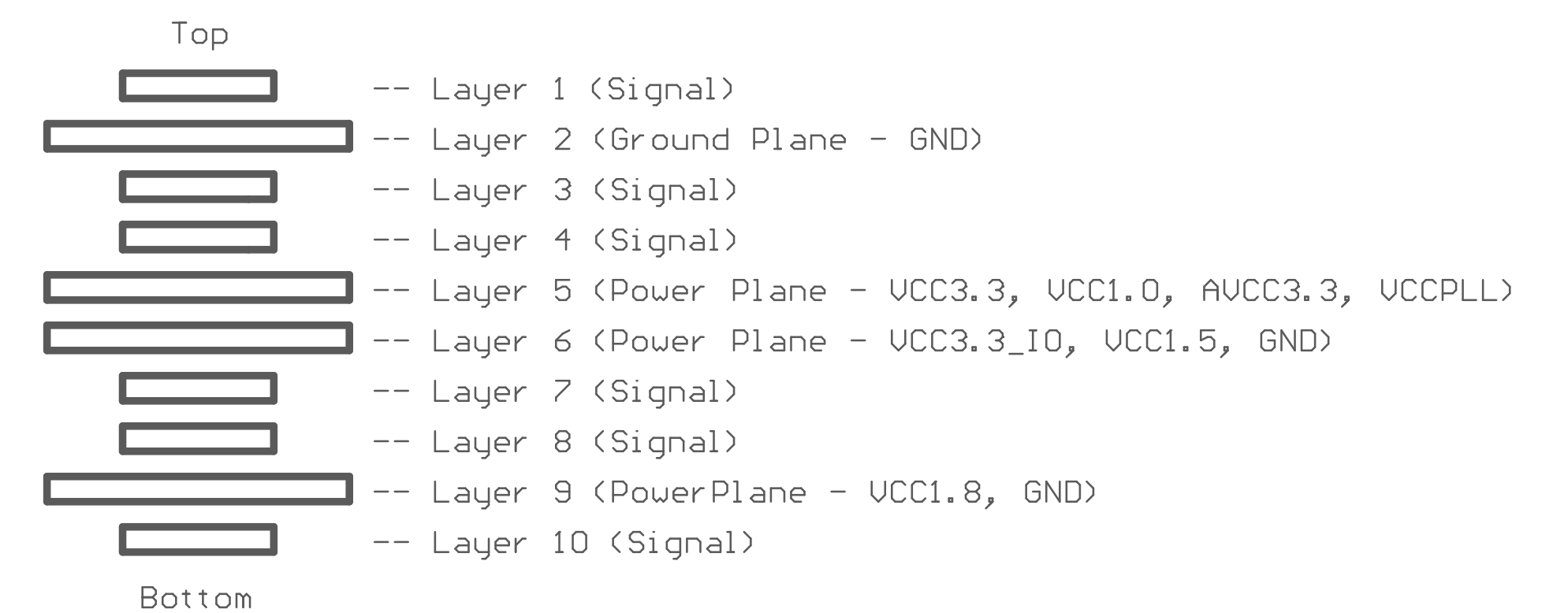
D

A

B

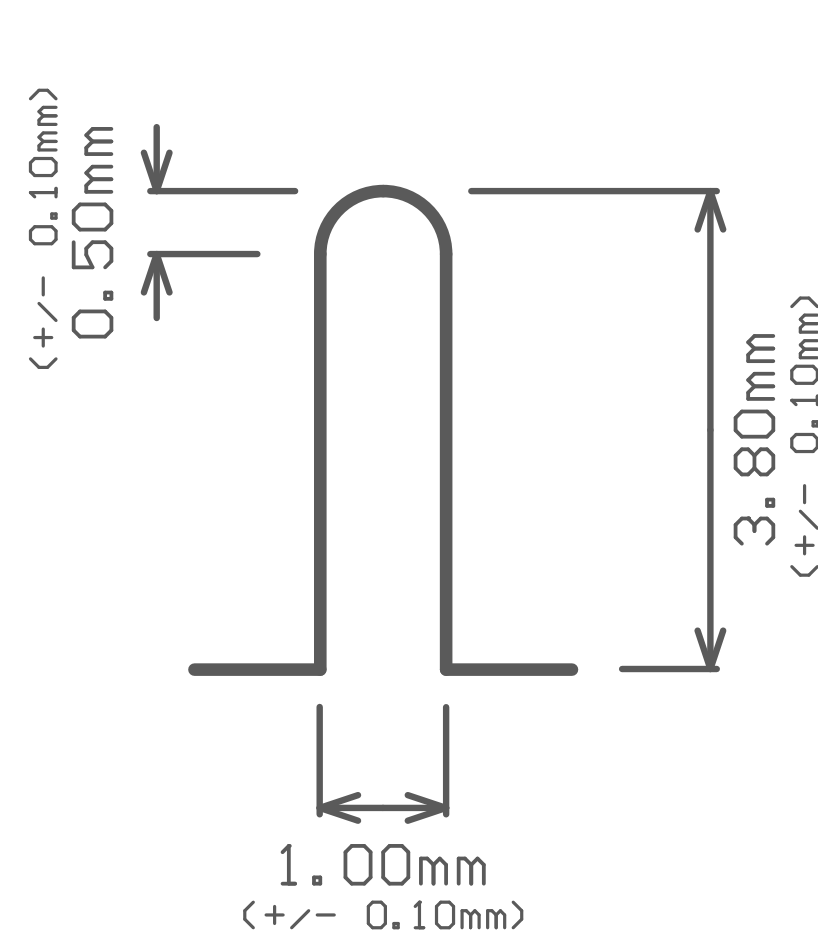
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Layer Stackup

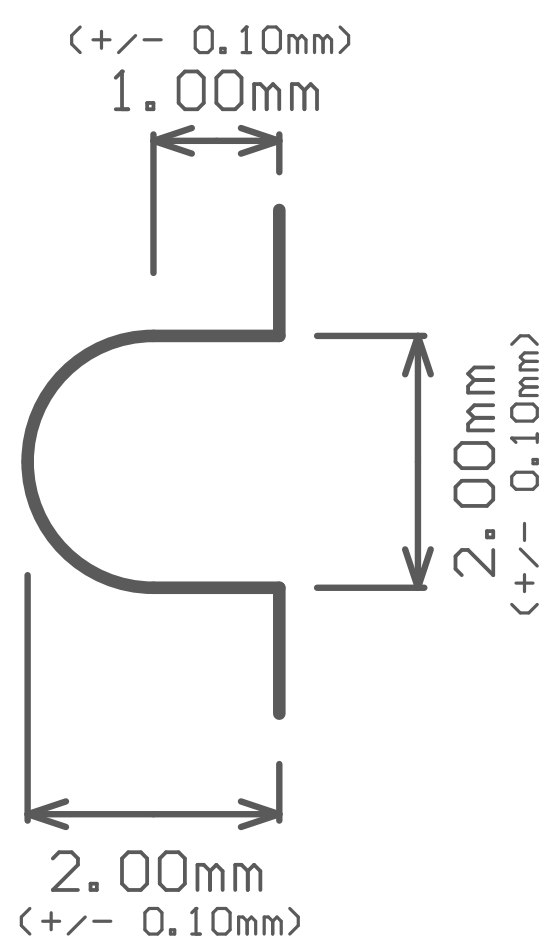


Univ. of Wisconsin—Madison Madison, WI 53706	ENGINEER: Vicente, M.	TITLE: ZYNQ—IPMC	
	PCB DESIGNER: Vicente, M.		
	DATE: 06JUN2019	PART NO.:	REV: revB1
	FILE NAME: ZYNQ_IPMC.PCBD0C	DWG NO:	SCALE: 1:1

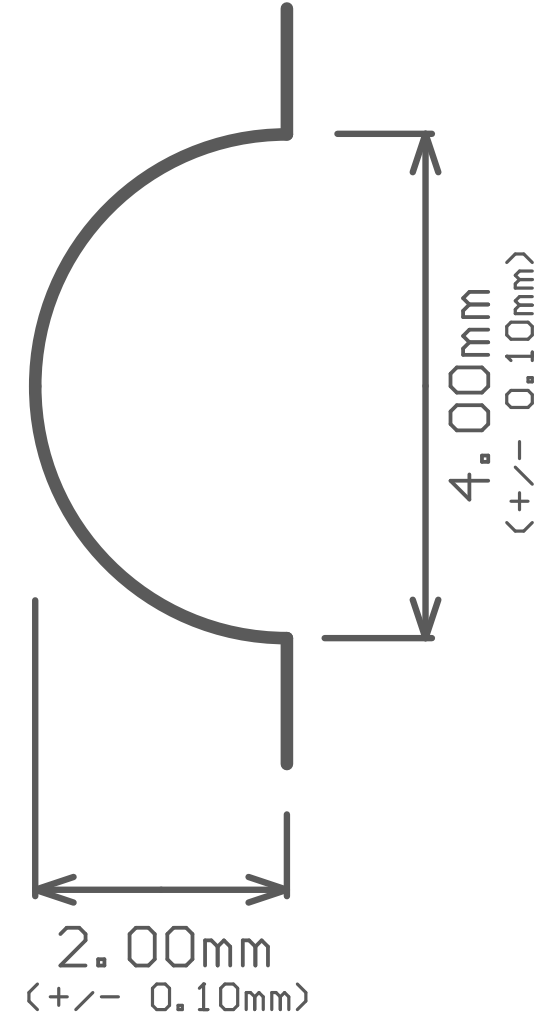
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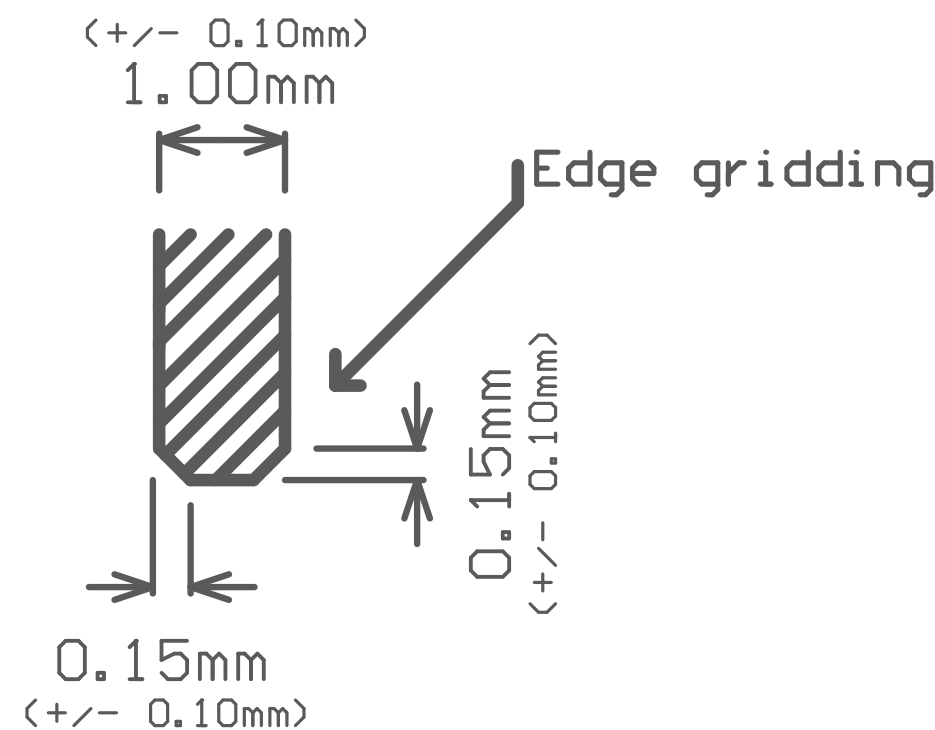
Detail 1



Detail 2



Detail 3

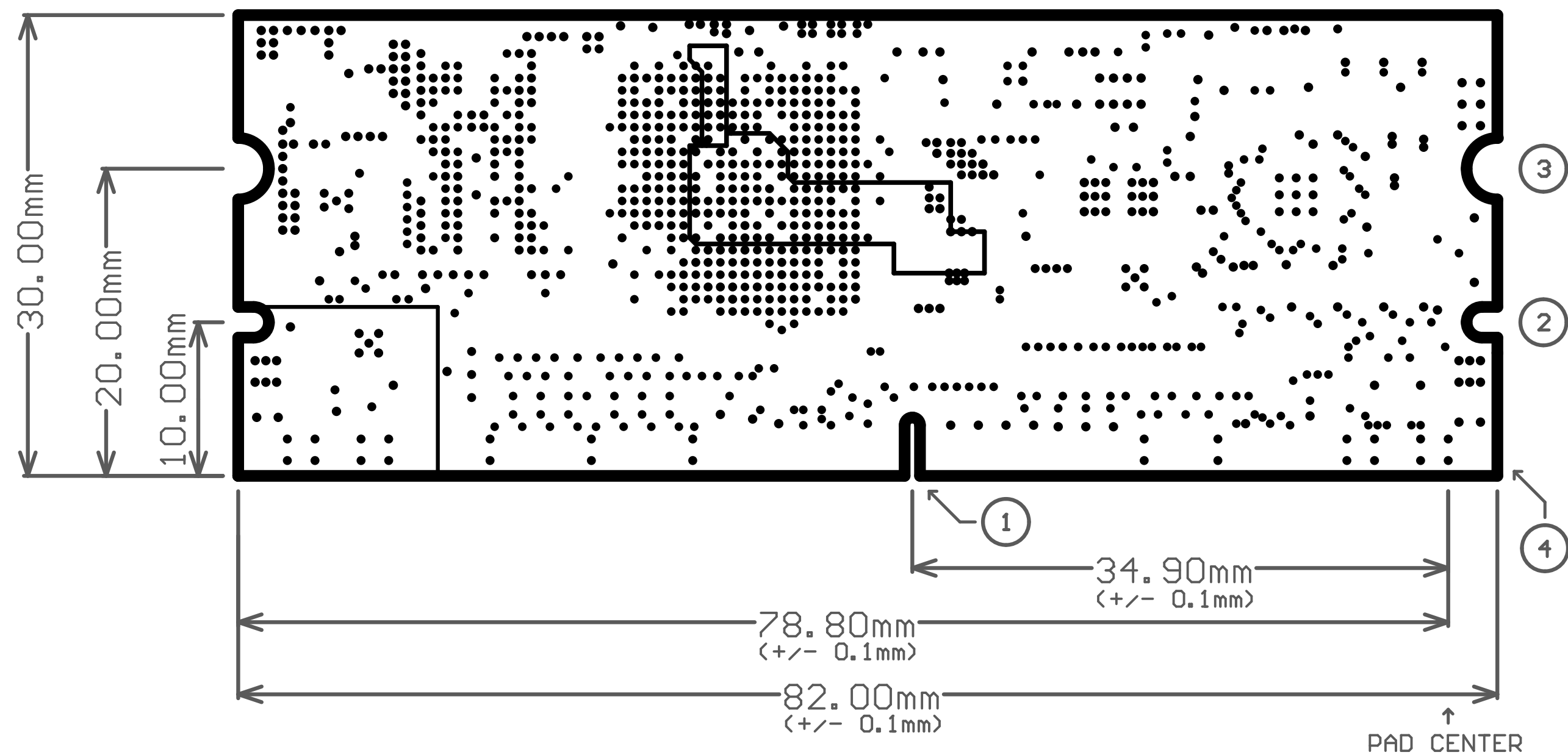


Detail 4
(PCB side view)

B

UW-IPMC MEZZANINE (revB)

Layer 5 - Power Plane (Copper, Mask)



C

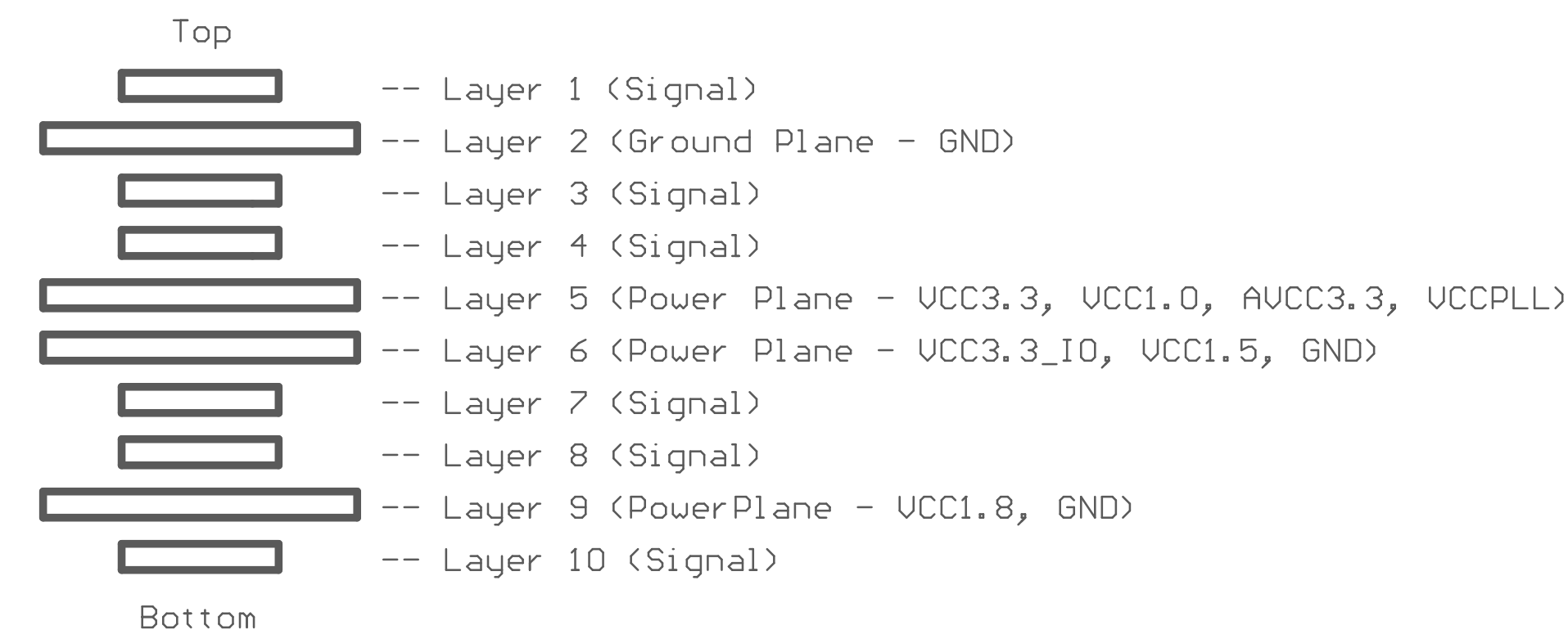
Specifications:

- Dielectric material is Tetrafunctional FR-4 with $T_g > 170\text{ }^{\circ}\text{C}$
- Overall thickness is 1.0mm $\pm 0.10\text{mm}$
- Board dimensions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
- Panelization
 - Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - Panels should contain fiducial marks for X,Y alignment
- Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
- All layers use 1/2 oz. copper (before plating)
- Holes:
 - Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - Drills are plated-through holes and their locations are given in a separate drill file.
- Finish:
 - Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - Overall board finish is immersion gold.
- Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
- Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimable, with maximum thickness of 3 mils
- Layers 2, 5, 6 and 9 are power planes and are INVERTED
- Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
- Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
- Combination of bow and twist shall not exceed 10 mils/inch along any direction
- Design origin is at the bottom-left corner of the PCB
- Testing:
 - All layers to undergo optical inspection (machine-based) of all layers before lamination
 - Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
- Locations in IPC-D-356A file are given in 2.4 English units
- South edge-to-edge connector details:
 - Details present in page 2 of the Molex 87783-0301 datasheet (included).

A

B

Layer Stackup

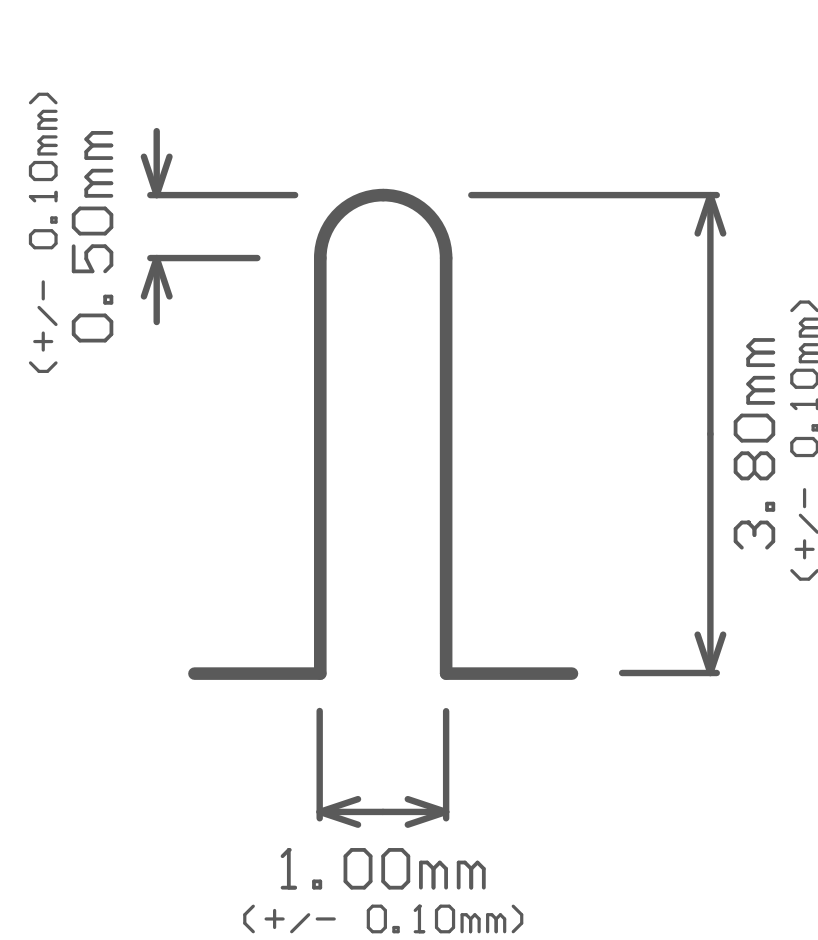


D

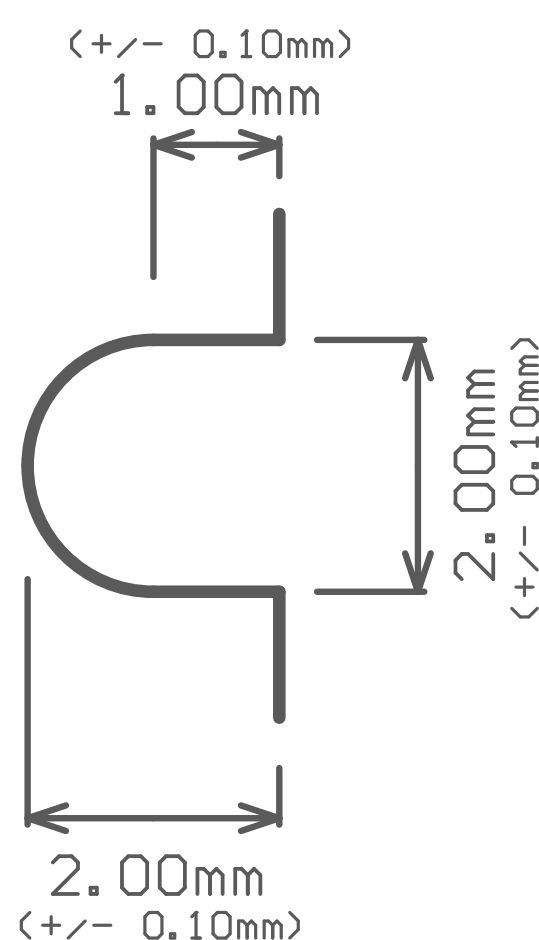
Univ. of Wisconsin—Madison Madison, WI 53706	ENGINEER: Vicente, M.	TITLE: ZYNQ—IPMC	
	PCB DESIGNER: Vicente, M.		
	DATE: 06JUN2019	PART NO.:	REV: revB1
	FILE NAME: ZYNQ_IPMC.PCBDOC	DWG NO:	SCALE: 1:1

D

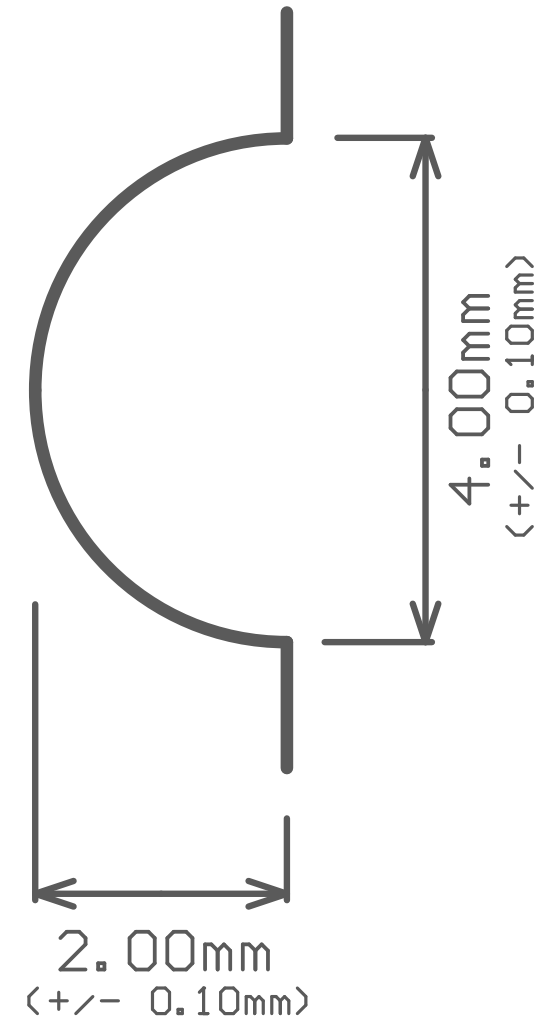
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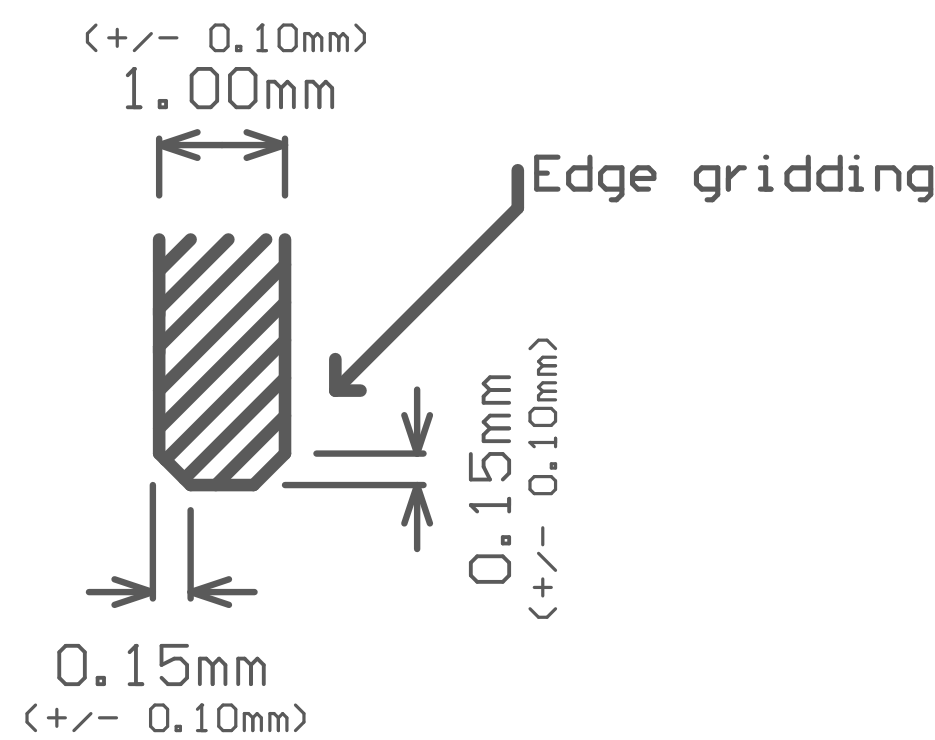
Detail 1



Detail 2



Detail 3

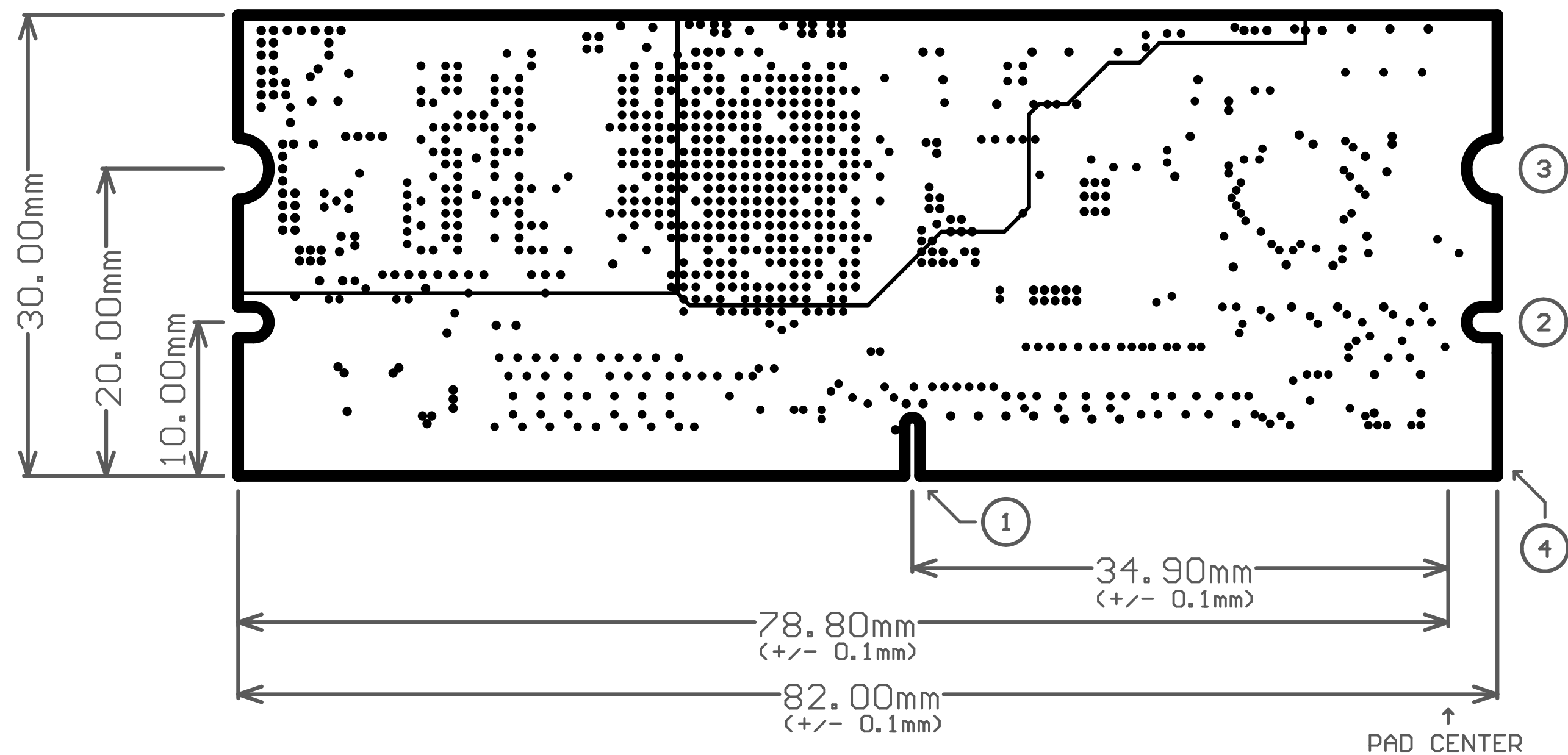


Detail 4
(PCB side view)

B

UW-IPMC MEZZANINE (revB)

Layer 6 - Power Plane (Copper, Mask)



C

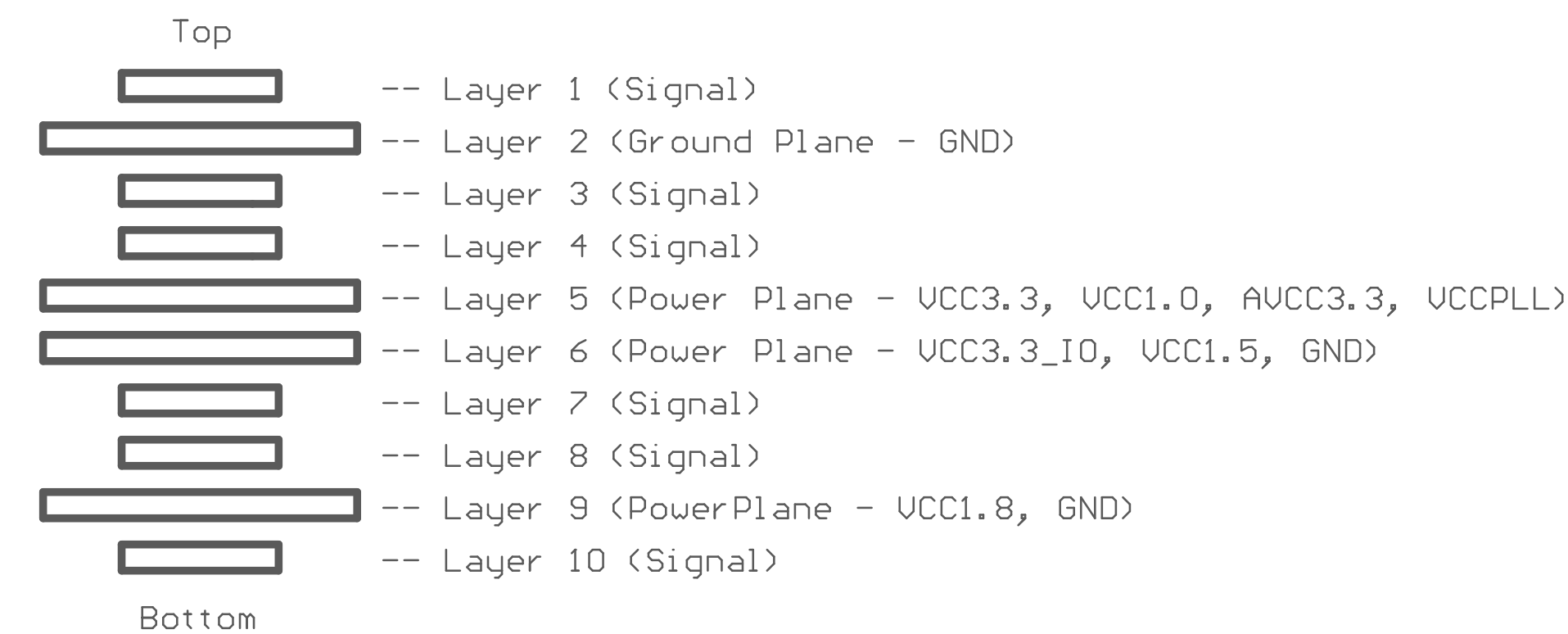
Specifications:

- Dielectric material is Tetrafunctional FR-4 with $T_g > 170\text{ C}$
- Overall thickness is 1.0mm $\pm 0.10\text{mm}$
- Board dimensions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
- Panelization
 - Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - Panels should contain fiducial marks for X,Y alignment
- Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
- All layers use 1/2 oz. copper (before plating)
- Holes:
 - Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - Drills are plated-through holes and their locations are given in a separate drill file.
- Finish:
 - Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - Overall board finish is immersion gold.
- Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
- Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils
- Layers 2, 5, 6 and 9 are power planes and are INVERTED
- Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
- Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
- Combination of bow and twist shall not exceed 10 mils/inch along any direction
- Design origin is at the bottom-left corner of the PCB
- Testing:
 - All layers to undergo optical inspection (machine-based) of all layers before lamination
 - Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
- Locations in IPC-D-356A file are given in 2.4 English units
- South edge-to-edge connector details:
 - Details present in page 2 of the Molex 87783-0301 datasheet (included).

A

B

Layer Stackup

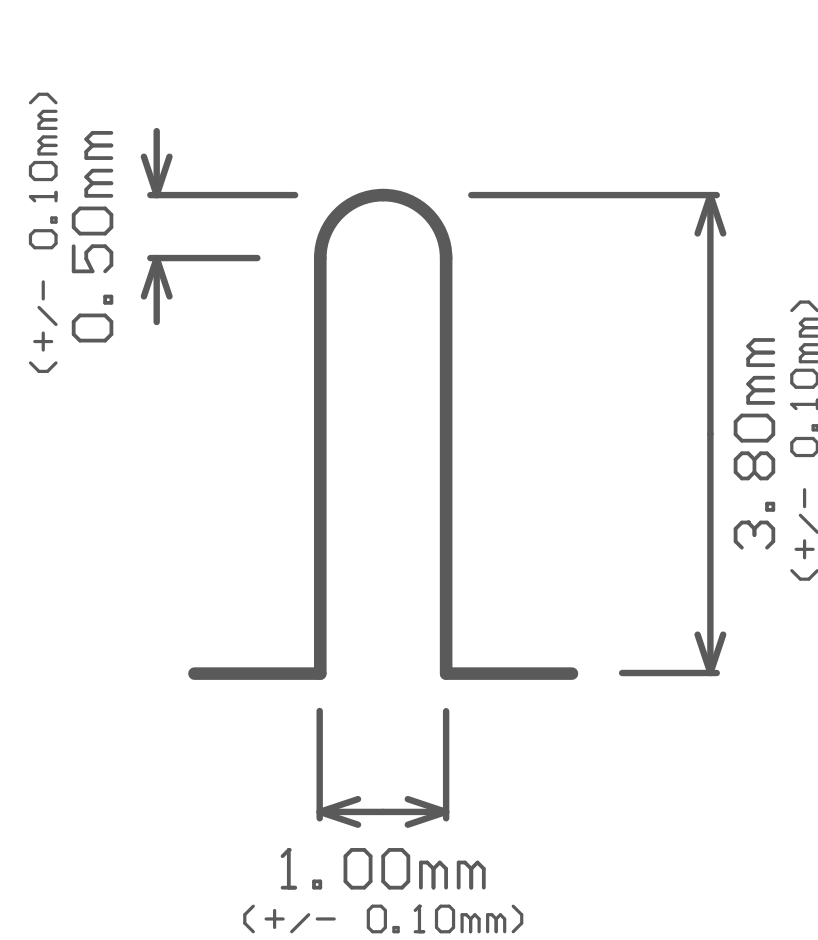


D

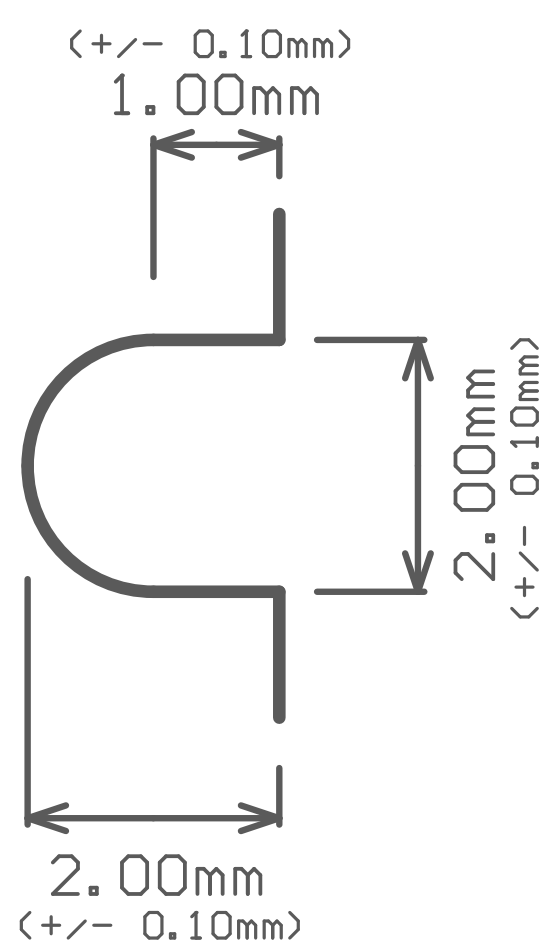
Univ. of Wisconsin—Madison Madison, WI 53706	ENGINEER: Vicente, M.	TITLE: ZYNQ—IPMC	
	PCB DESIGNER: Vicente, M.		
	DATE: 06JUN2019	PART NO.:	REV: revB1
	FILE NAME: ZYNQ_IPMC.PCBDOC	DWG NO:	SCALE: 1:1

D

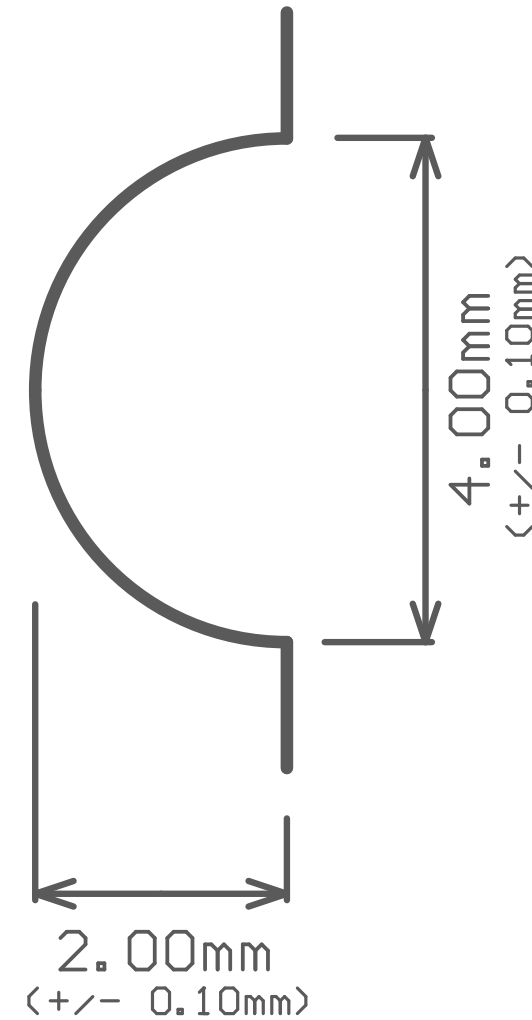
A



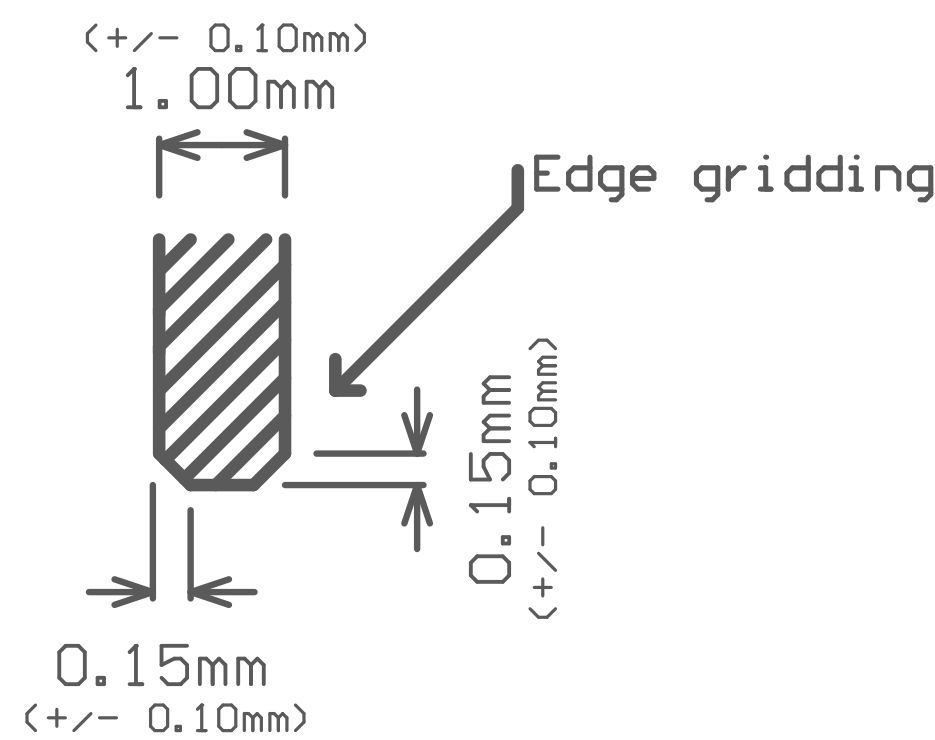
Detail 1



Detail 2



Detail 3

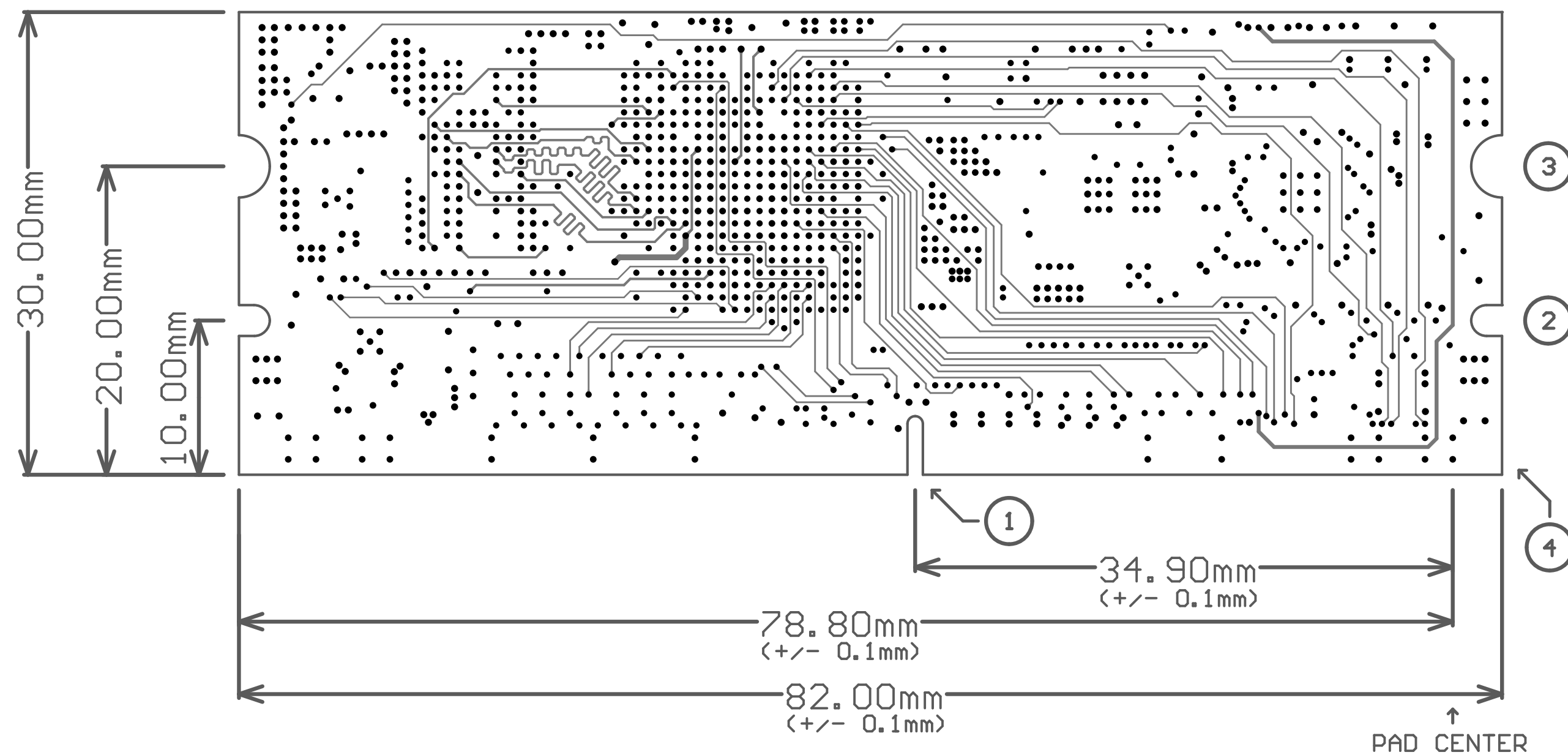


Detail 4
(PCB side view)

B

UW-IPMC MEZZANINE (revB)

Layer 7 - Signal (Copper)



C

D

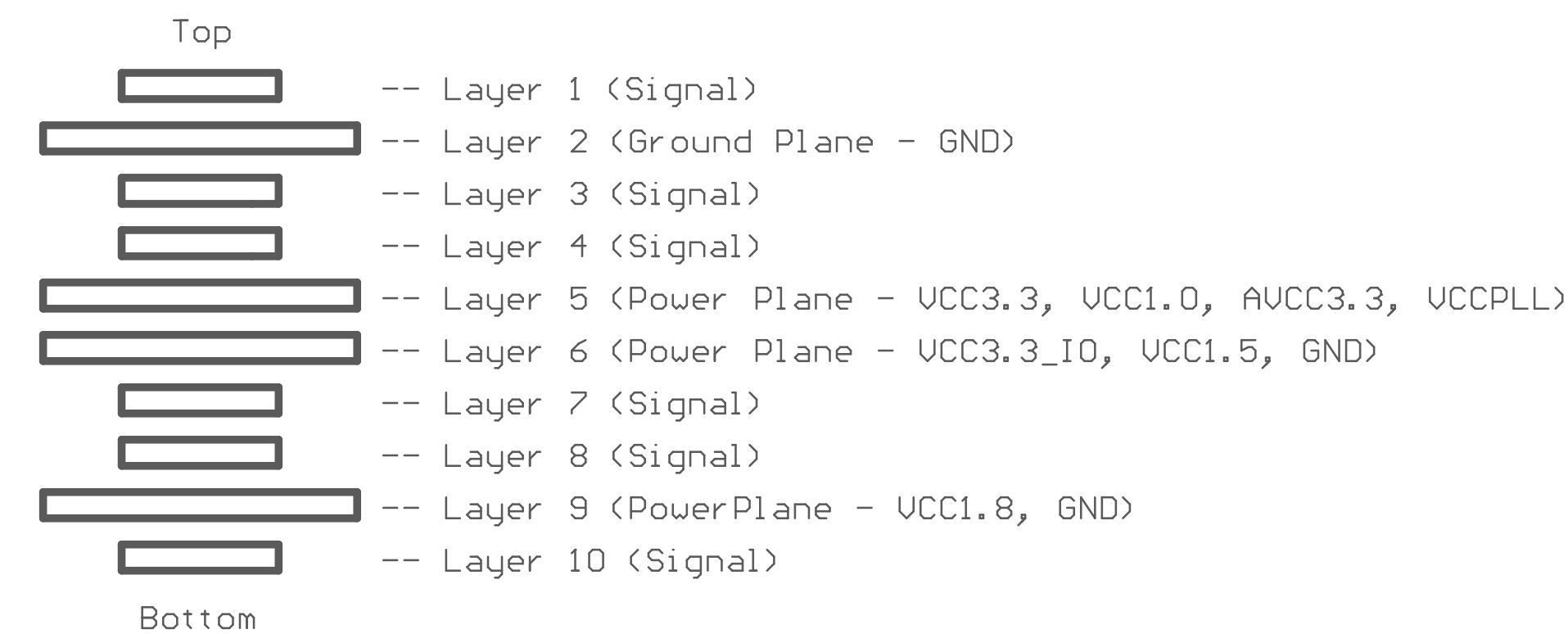
Specifications:

- Dielectric material is Tetrafunctional FR-4 with $T_g > 170\text{ }^{\circ}\text{C}$
- Overall thickness is 1.0mm $\pm 0.10\text{mm}$
- Board dimensions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
- Panelization
 - Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - Panels should contain fiducial marks for X,Y alignment
- Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
- All layers use 1/2 oz. copper (before plating)
- Holes:
 - Hole diameters are given as after plating $\pm 3\text{ mils}$, except as noted on drill drawing
 - Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - Drills are plated-through holes and their locations are given in a separate drill file.
- Finish:
 - Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - Overall board finish is immersion gold.
- Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
- Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photomailable, with maximum thickness of 3 mils
- Layers 2, 5, 6 and 9 are power planes and are INVERTED
- Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
- Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
- Combination of bow and twist shall not exceed 10 mils/inch along any direction
- Design origin is at the bottom-left corner of the PCB
- Testing:
 - All layers to undergo optical inspection (machine-based) of all layers before lamination
 - Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
- Locations in IPC-D-356A file are given in 2.4 English units
- South edge-to-edge connector details:
 - Details present in page 2 of the Molex 87783-0301 datasheet (included).

A

B

Layer Stackup



Univ. of Wisconsin—Madison Madison, WI 53706	ENGINEER: Vicente, M.	TITLE: ZYNQ—IPMC	
	PCB DESIGNER: Vicente, M.		
	DATE: 06JUN2019	PART NO.:	REV: revB1
	FILE NAME: ZYNQ_IPMC.PCBDOC	DWG NO:	SCALE: 1:1

D

A

B

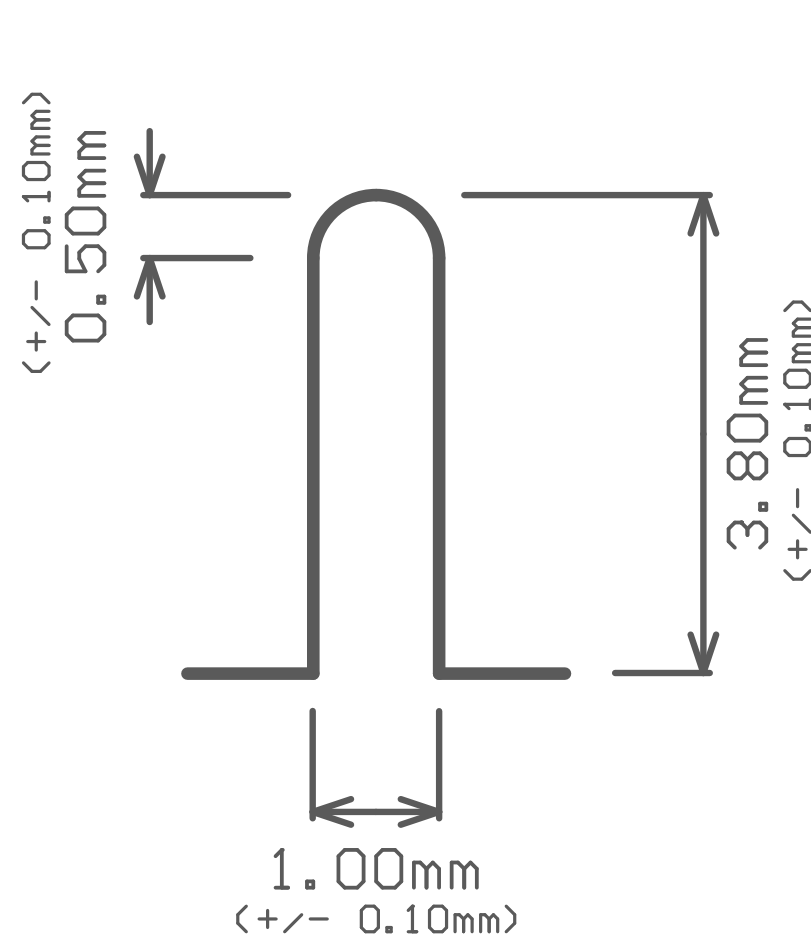
C

D

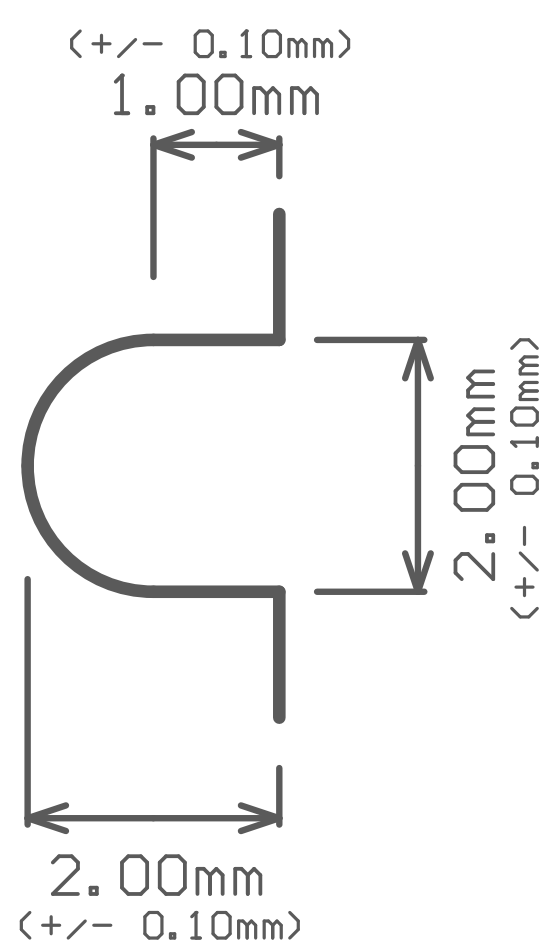
A

B

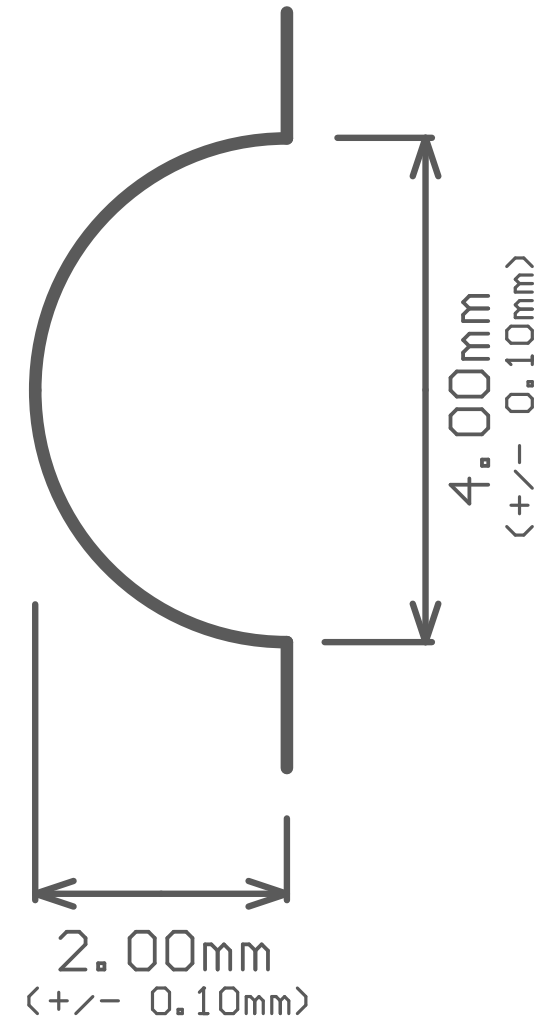
D



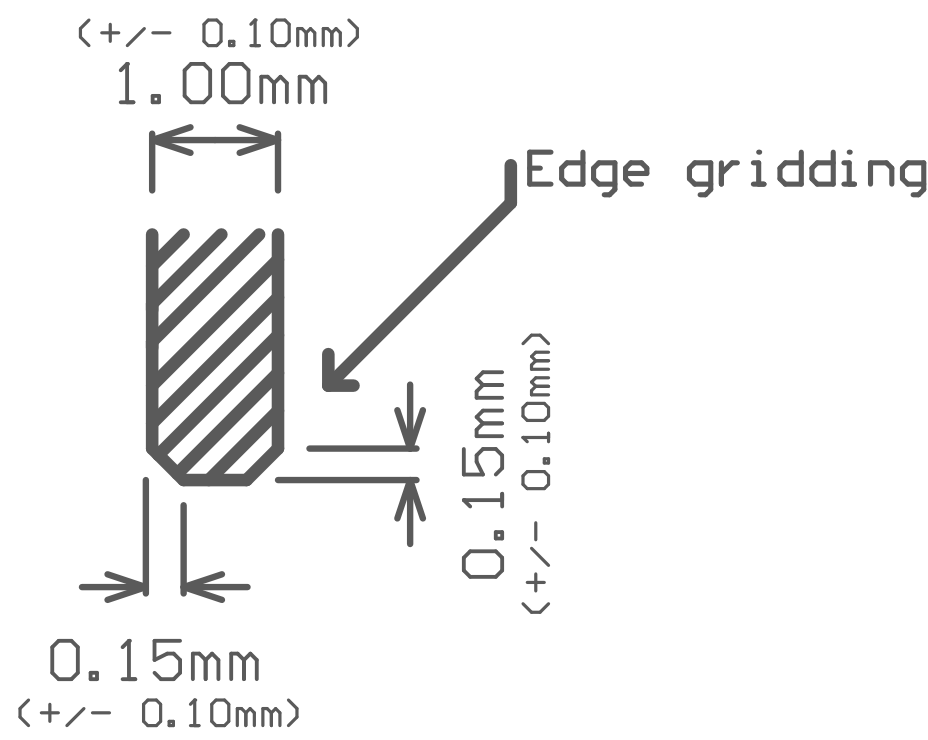
Detail 1



Detail 2



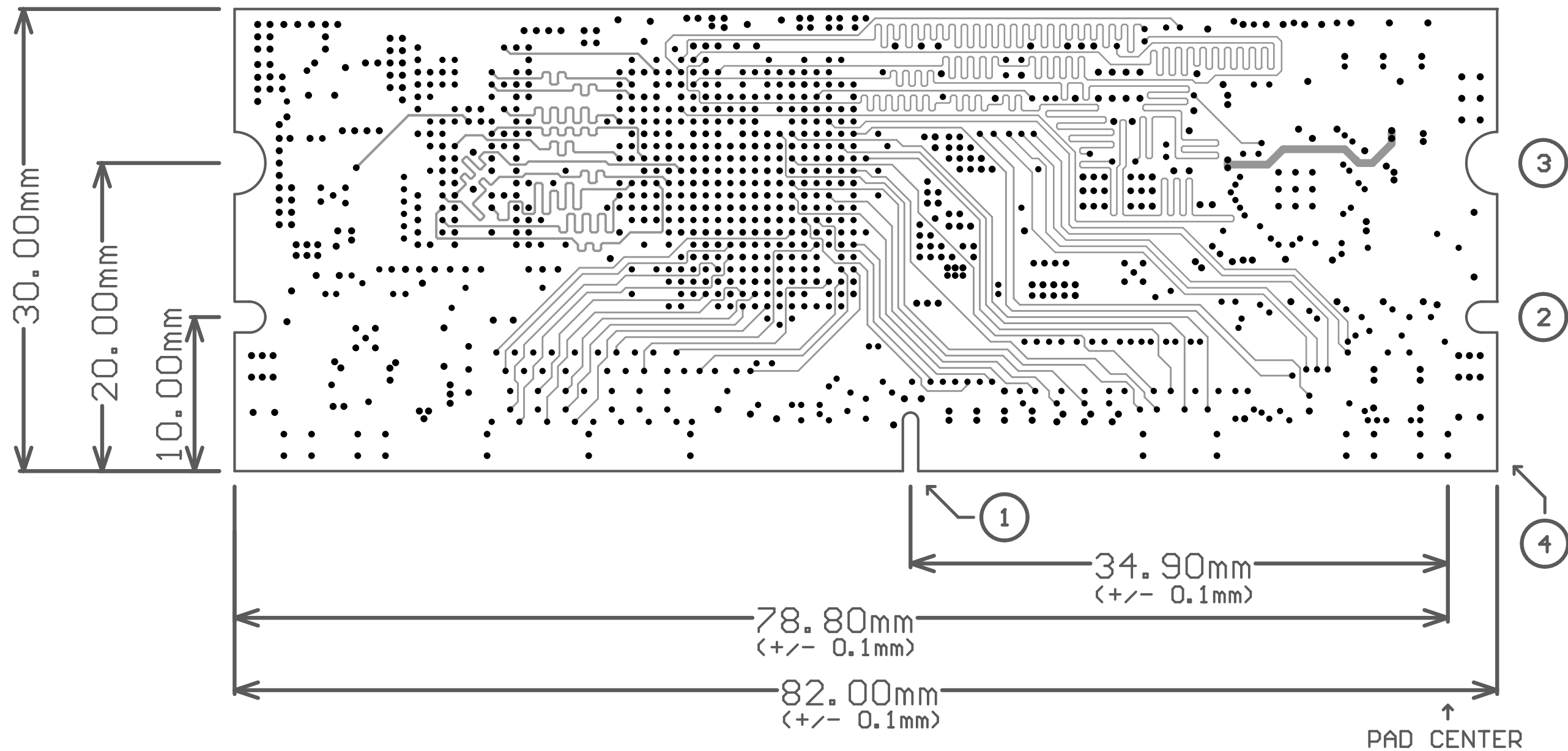
Detail 3



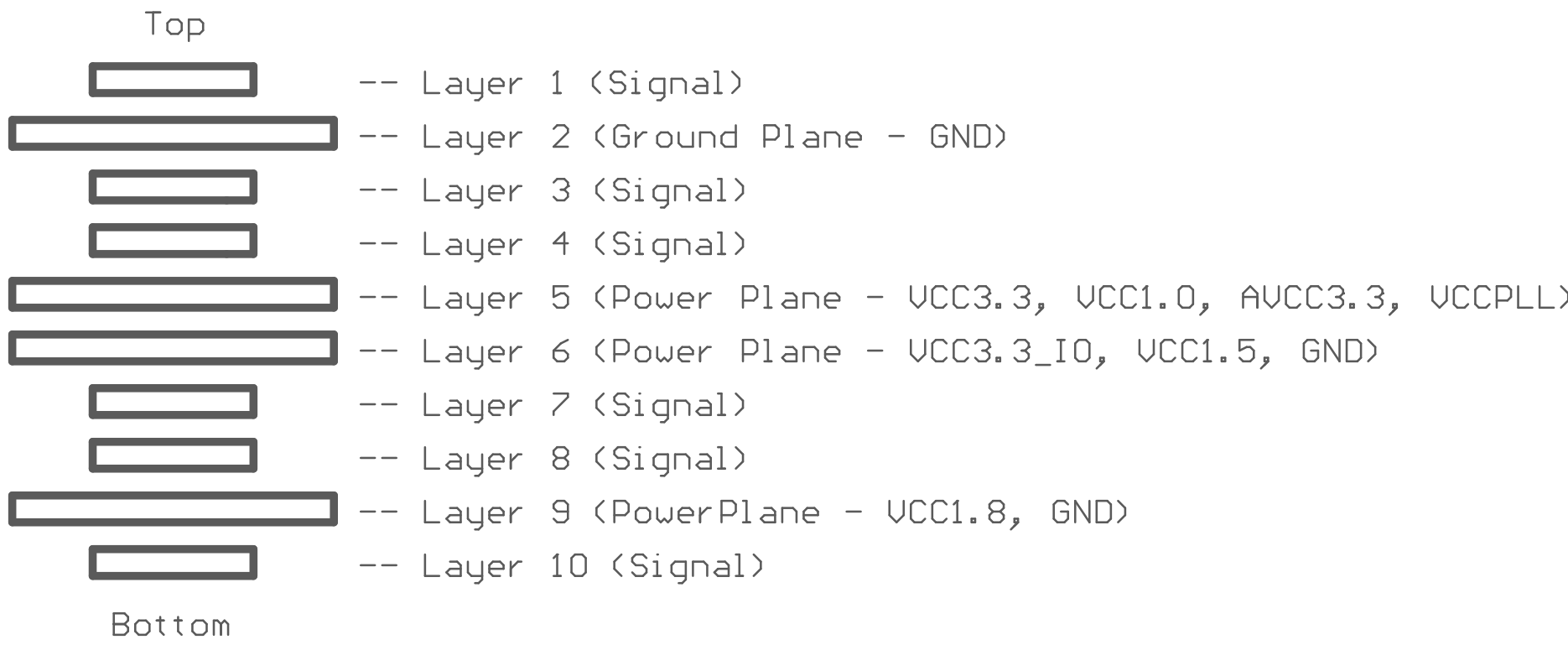
Detail 4
(PCB side view)

UW-IPMC MEZZANINE (revB)

Layer 8 - Signal (Copper)

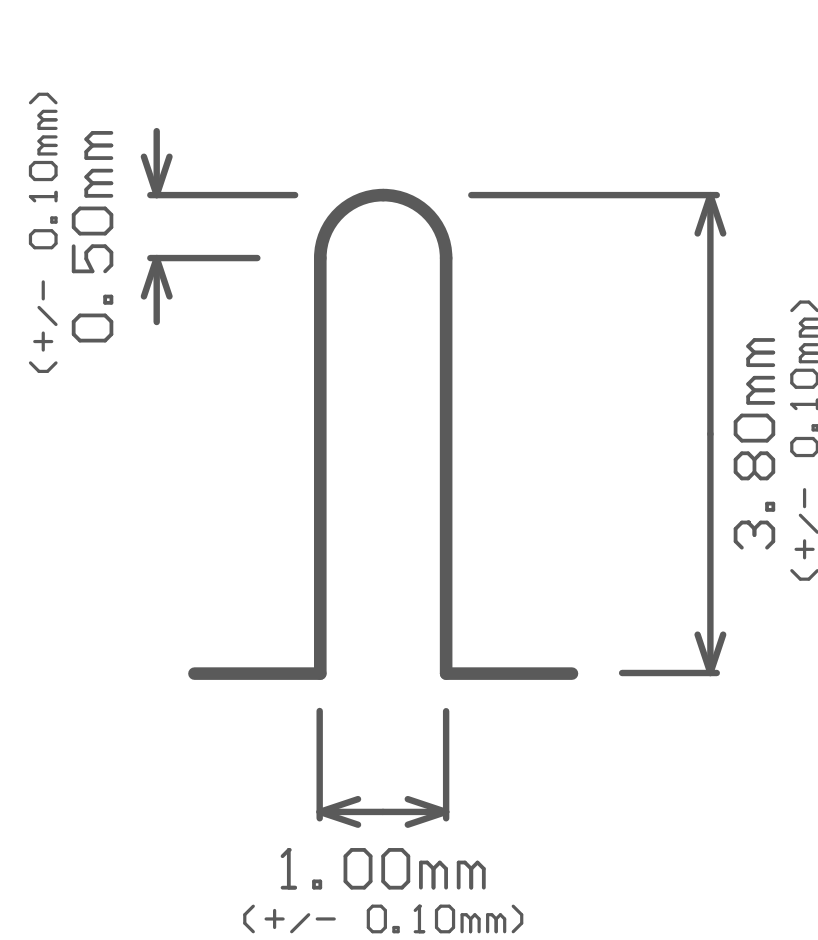


Layer Stackup

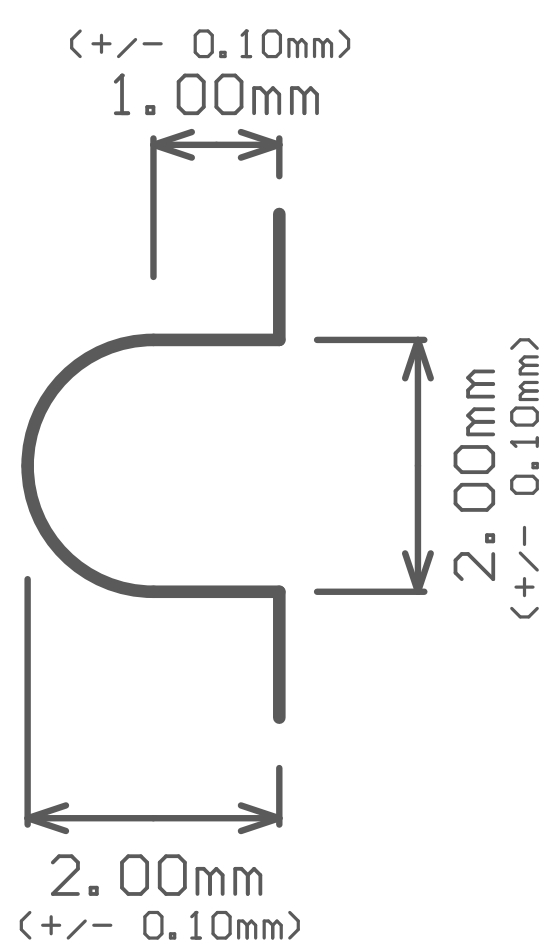


Univ. of Wisconsin—Madison Madison, WI 53706	ENGINEER: Vicente, M.	TITLE: ZYNQ—IPMC	
	PCB DESIGNER: Vicente, M.		
	DATE: 06JUN2019	PART NO.:	REV: revB1
	FILE NAME: ZYNQ_IPMC.PCBDOC	DWG NO:	SCALE: 1:1

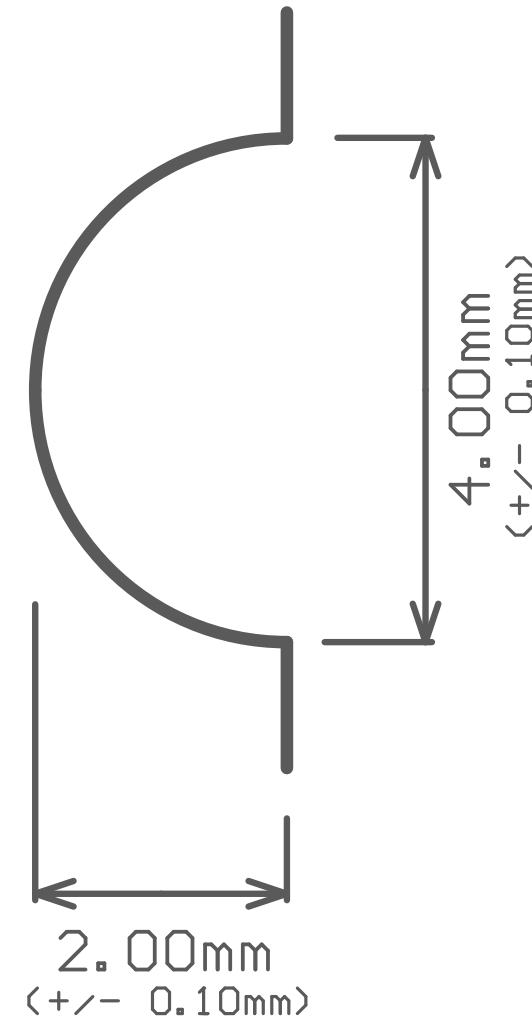
A



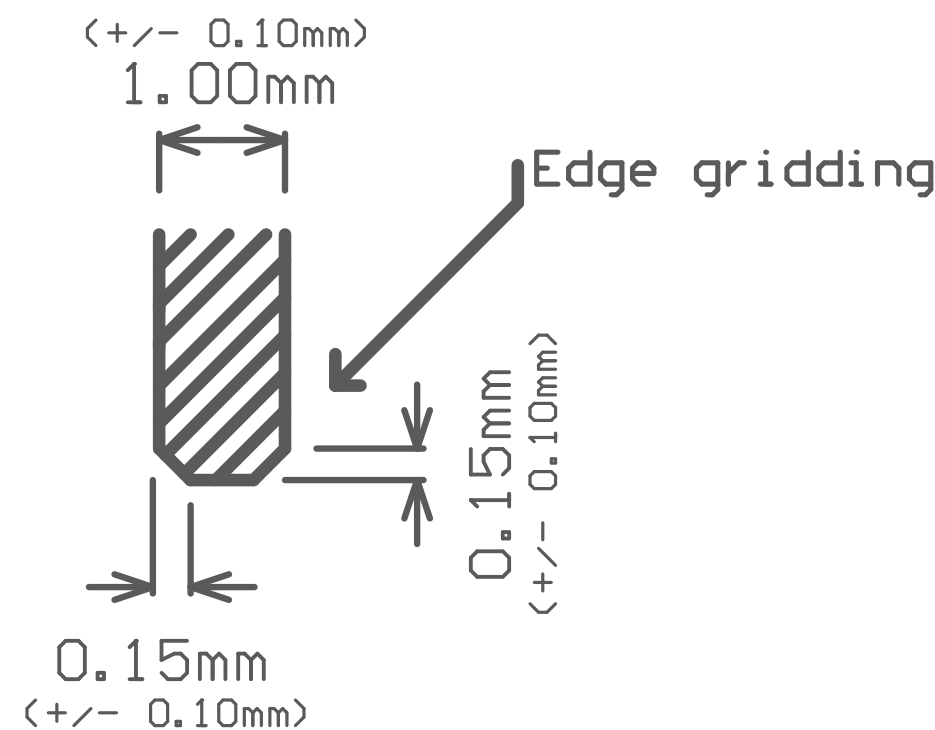
Detail 1



Detail 2



Detail 3

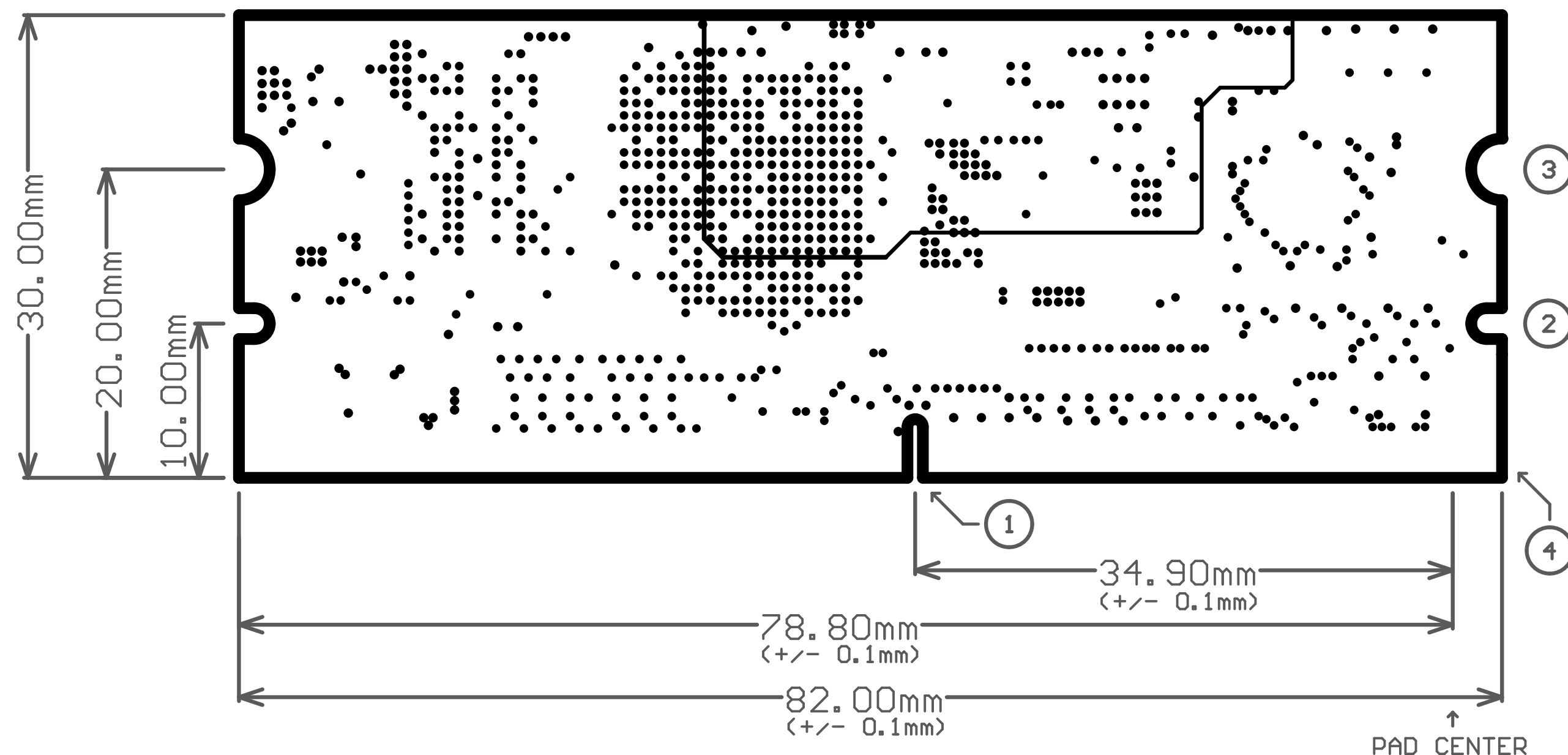


Detail 4
(PCB side view)

B

UW-IPMC MEZZANINE (revB)

Layer 9 - Power Plane (Copper, Mask)



C

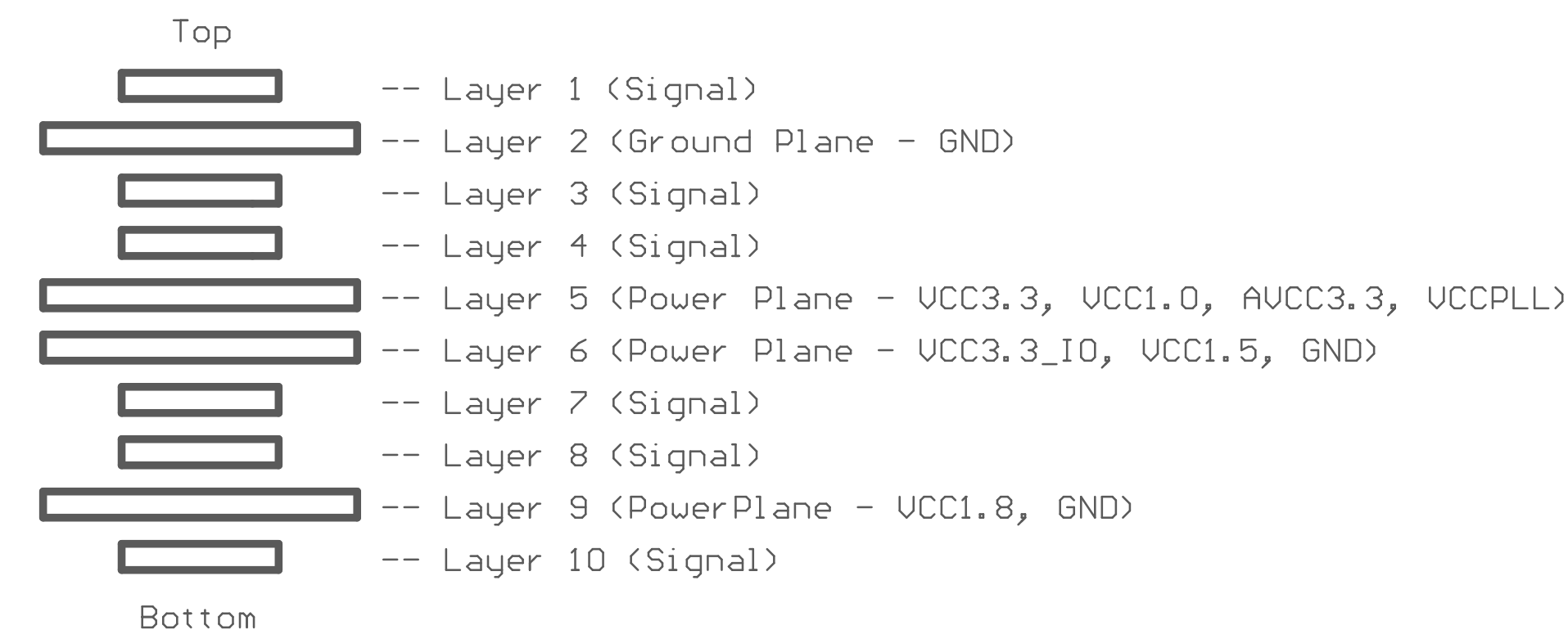
Specifications:

- Dielectric material is Tetrafunctional FR-4 with $T_g > 170\text{ }^{\circ}\text{C}$
- Overall thickness is 1.0mm $\pm 0.10\text{mm}$
- Board dimensions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
- Panelization
 - Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - Panels should contain fiducial marks for X,Y alignment
- Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
- All layers use 1/2 oz. copper (before plating)
- Holes:
 - Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - Drills are plated-through holes and their locations are given in a separate drill file.
- Finish:
 - Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - Overall board finish is immersion gold.
- Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
- Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils
- Layers 2, 5, 6 and 9 are power planes and are INVERTED
- Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
- Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
- Combination of bow and twist shall not exceed 10 mils/inch along any direction
- Design origin is at the bottom-left corner of the PCB
- Testing:
 - All layers to undergo optical inspection (machine-based) of all layers before lamination
 - Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
- Locations in IPC-D-356A file are given in 2.4 English units
- South edge-to-edge connector details:
 - Details present in page 2 of the Molex 87783-0301 datasheet (included).

A

B

Layer Stackup



D

Univ. of Wisconsin—Madison Madison, WI 53706	ENGINEER: Vicente, M.	TITLE: ZYNQ—IPMC	
	PCB DESIGNER: Vicente, M.		
	DATE: 06JUN2019	PART NO.:	REV: revB1
	FILE NAME: ZYNQ_IPMC.PCBDOC	DWG NO:	SCALE: 1:1

D

A

B

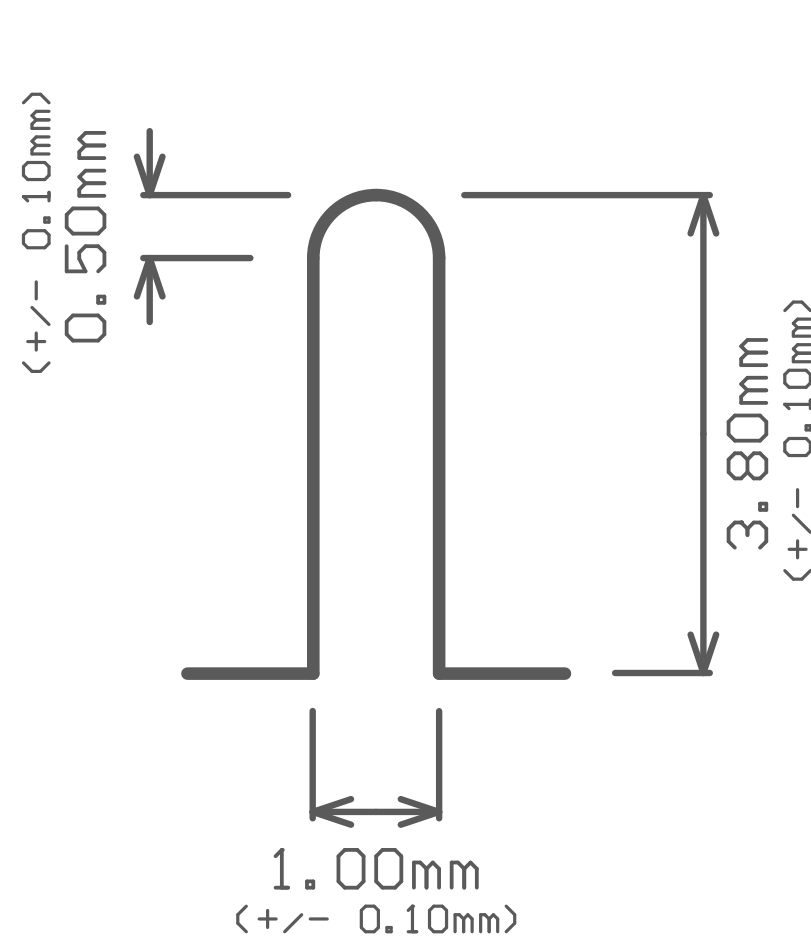
C

D

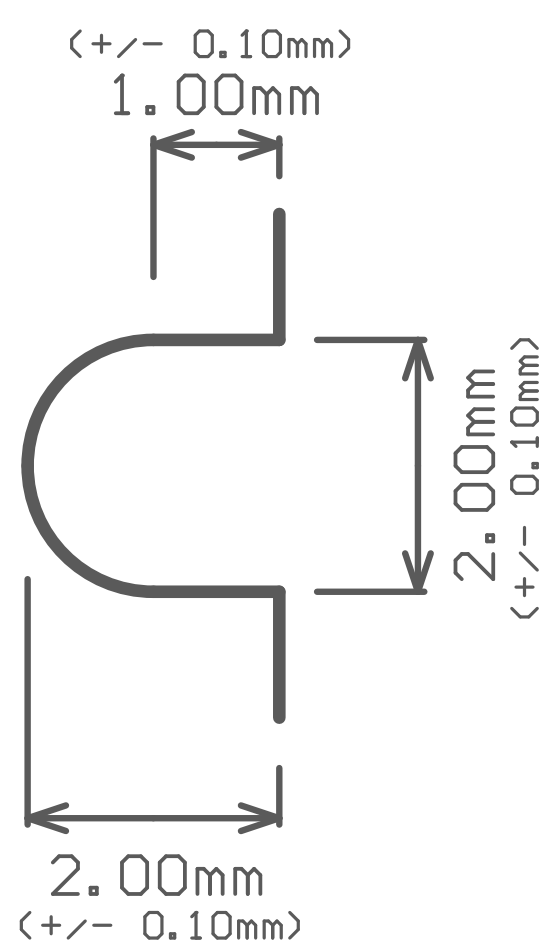
A

B

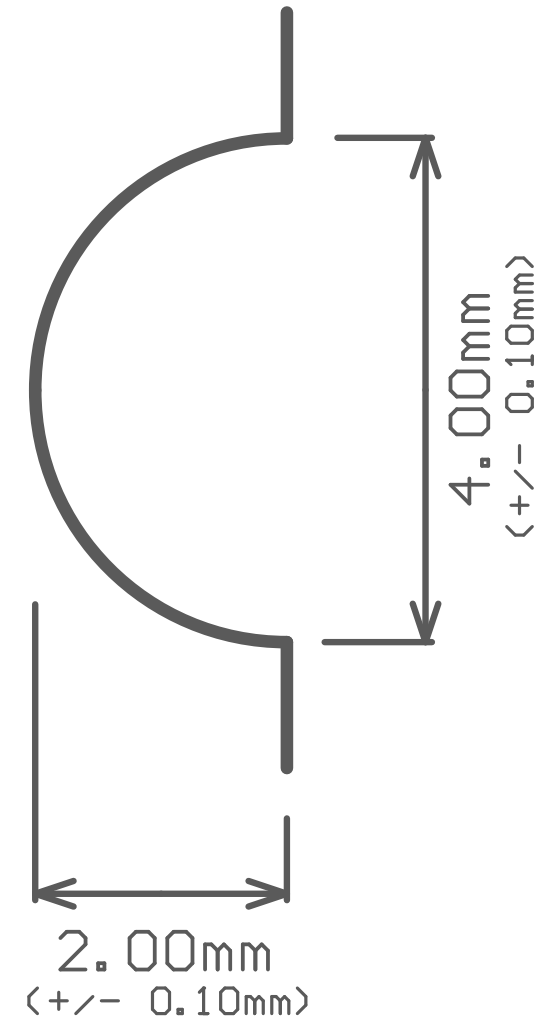
D



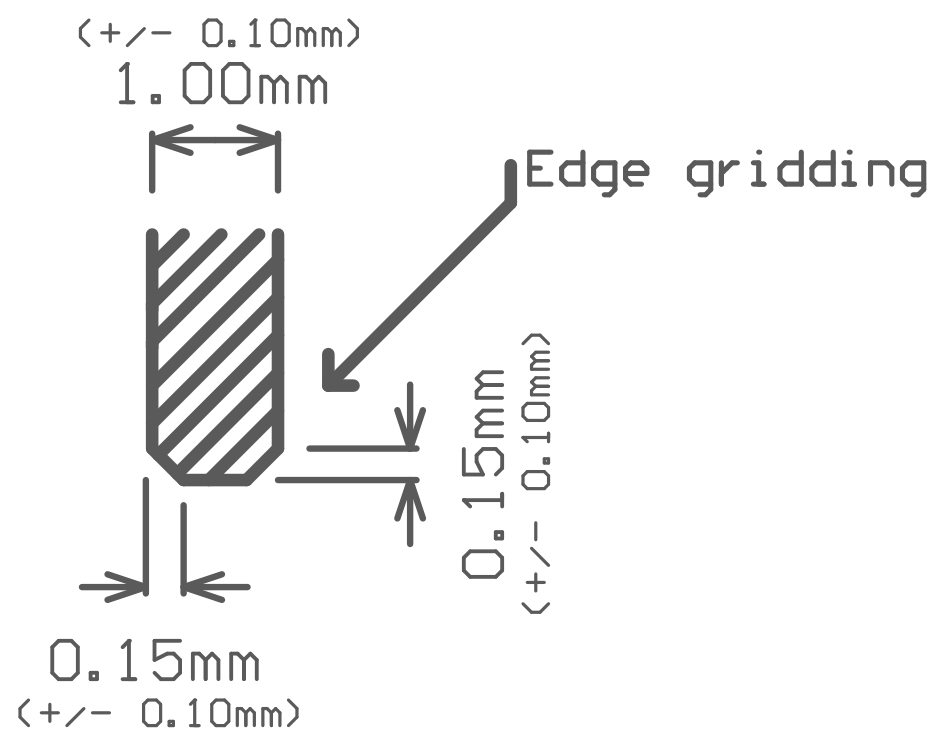
Detail 1



Detail 2



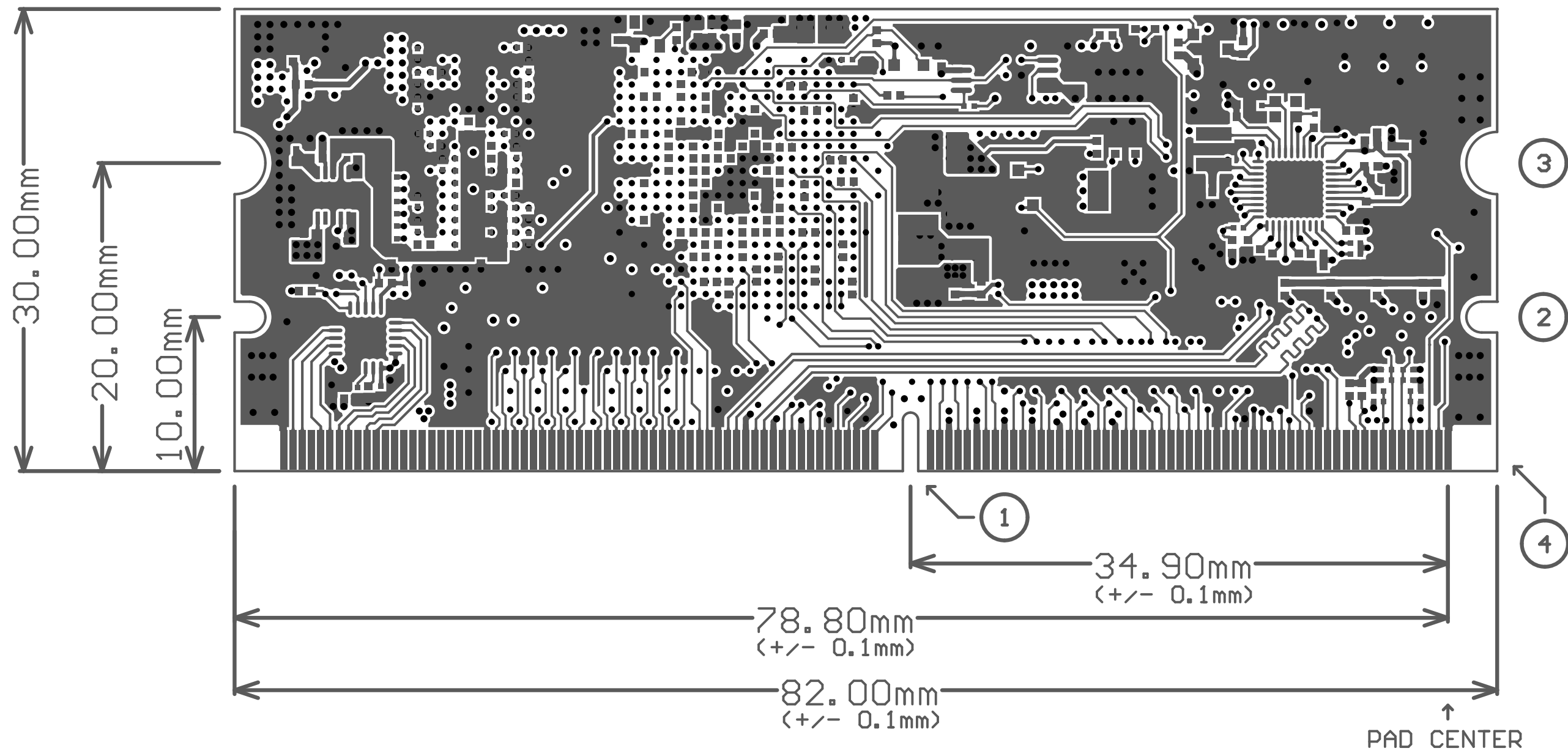
Detail 3



Detail 4
(PCB side view)

UW-IPMC MEZZANINE (revB)

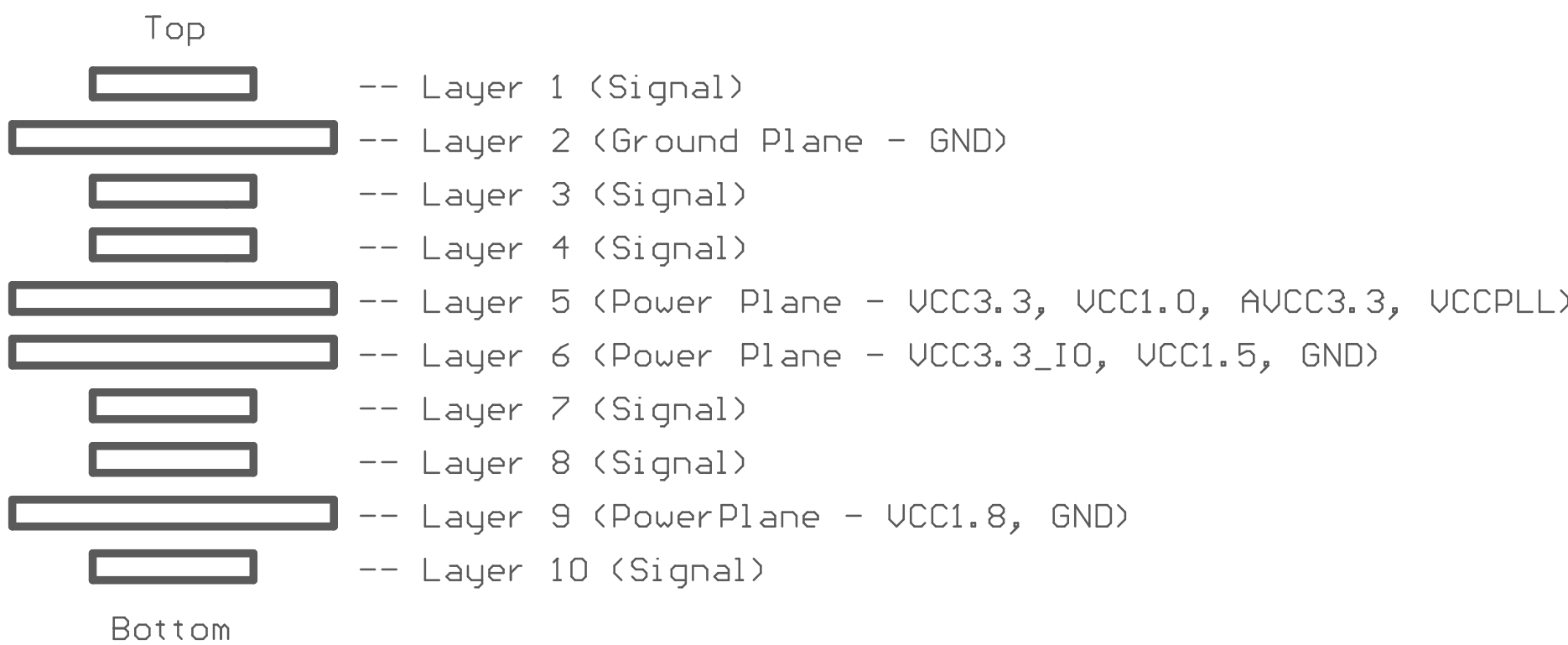
Layer 10 - Signal (Copper)



Specifications:

- Dielectric material is Tetrafunctional FR-4 with $T_g > 170\text{ C}$
- Overall thickness is 1.0mm $\pm 0.10\text{mm}$
- Board dimensions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
- Panelization
 - Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - Panels should contain fiducial marks for X,Y alignment
- Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
- All layers use 1/2 oz. copper (before plating)
- Holes:
 - Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - Drills are plated-through holes and their locations are given in a separate drill file.
- Finish:
 - Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - Overall board finish is immersion gold.
- Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
- Red colored solder mask shall be applied to both top and bottom surfaces.
Mask shall be photomaskable, with maximum thickness of 3 mils
- Layers 2, 5, 6 and 9 are power planes and are INVERTED
- Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
- Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
- Combination of bow and twist shall not exceed 10 mils/inch along any direction
- Design origin is at the bottom-left corner of the PCB
- Testing:
 - All layers to undergo optical inspection (machine-based) of all layers before lamination
 - Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
- Locations in IPC-D-356A file are given in 2.4 English units
- South edge-to-edge connector details:
 - Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup



Univ. of Wisconsin—Madison Madison, WI 53706	ENGINEER: Vicente, M.	TITLE: ZYNQ—IPMC	
	PCB DESIGNER: Vicente, M.		
	DATE: 06JUN2019	PART NO.:	REV: revB1
	FILE NAME: ZYNQ_IPMC.PCBDOC	DWG NO:	SCALE: 1:1

A

B

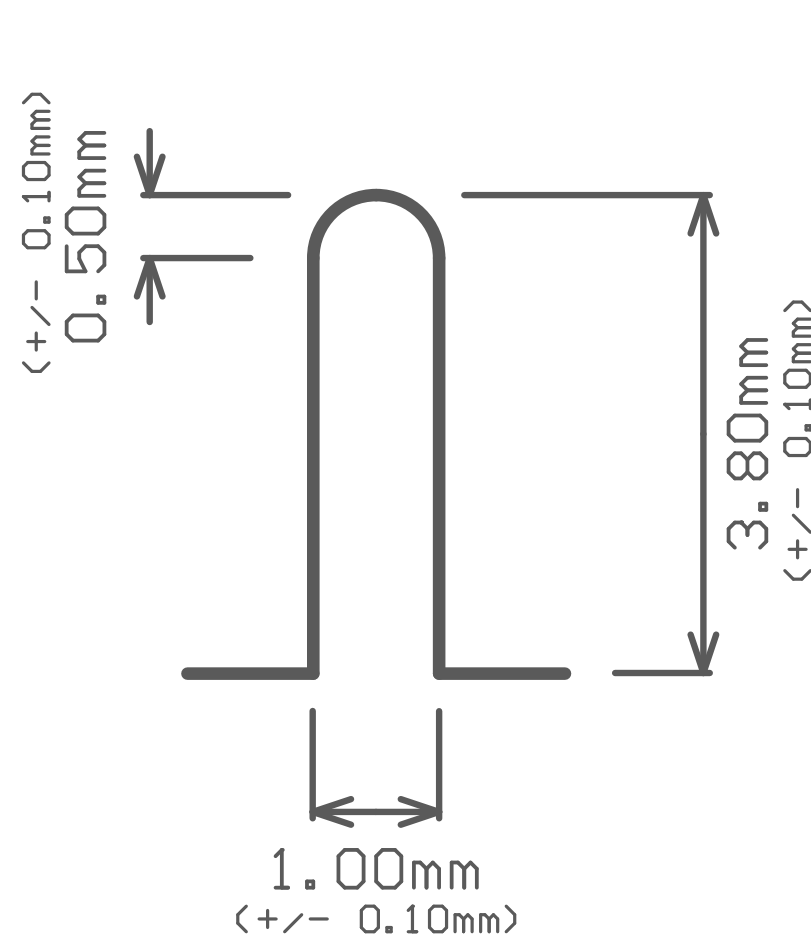
C

D

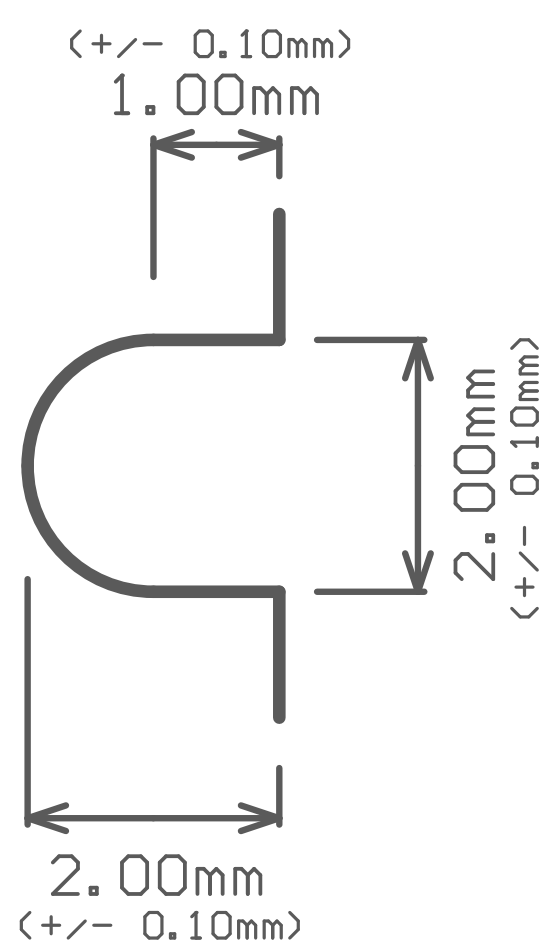
A

B

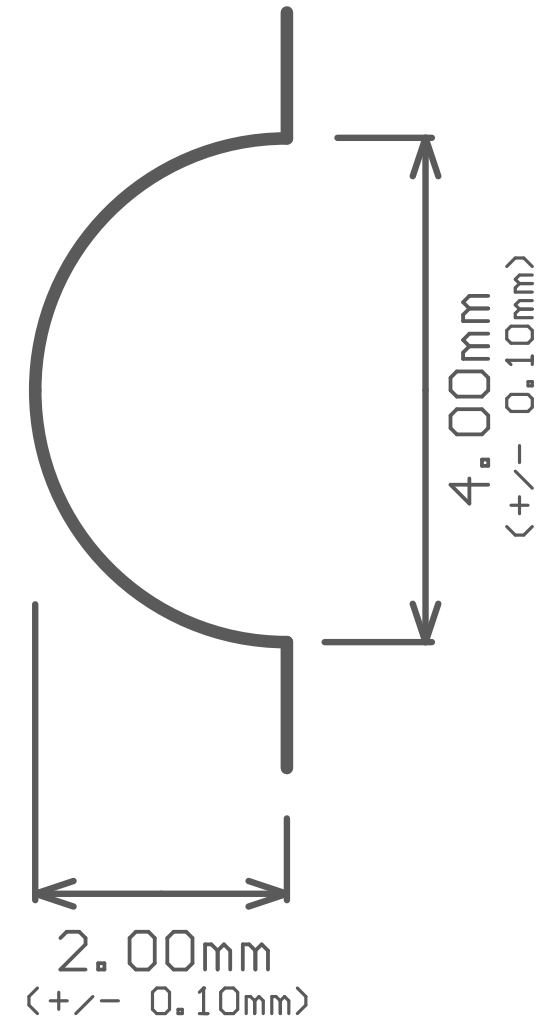
D



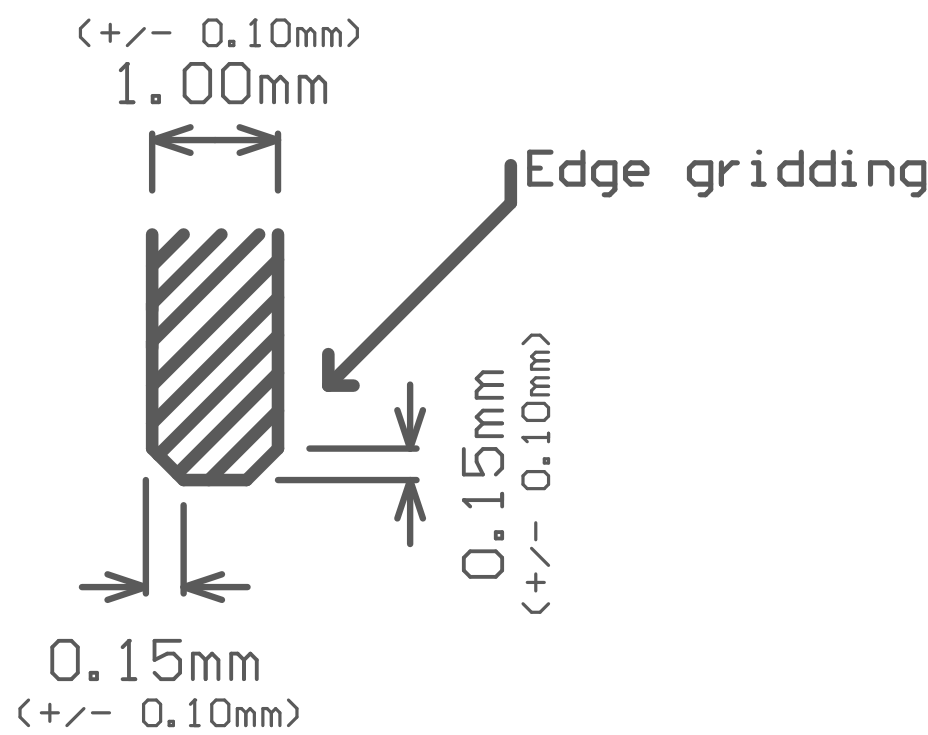
Detail 1



Detail 2



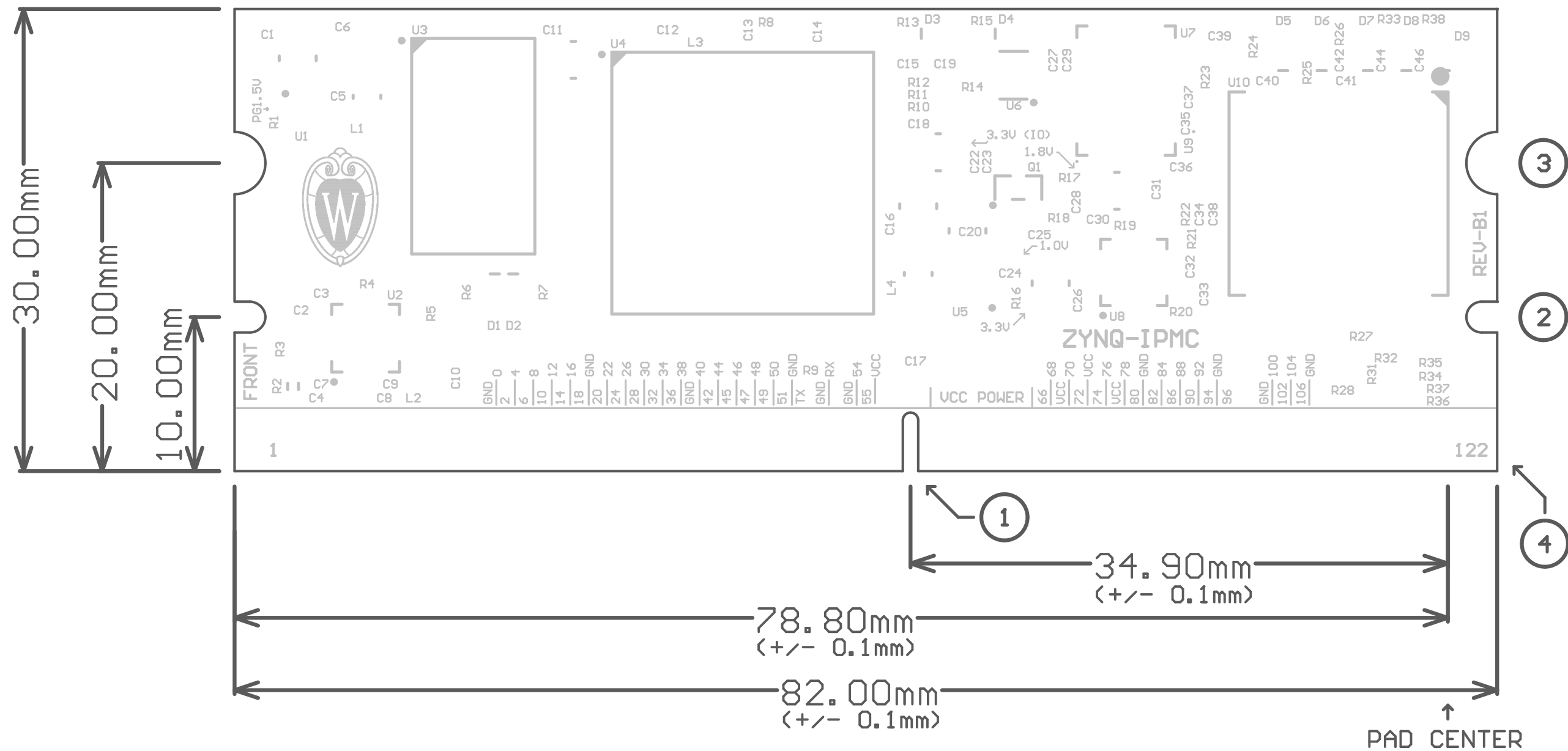
Detail 3



Detail 4
(PCB side view)

UW-IPMC MEZZANINE (revB)

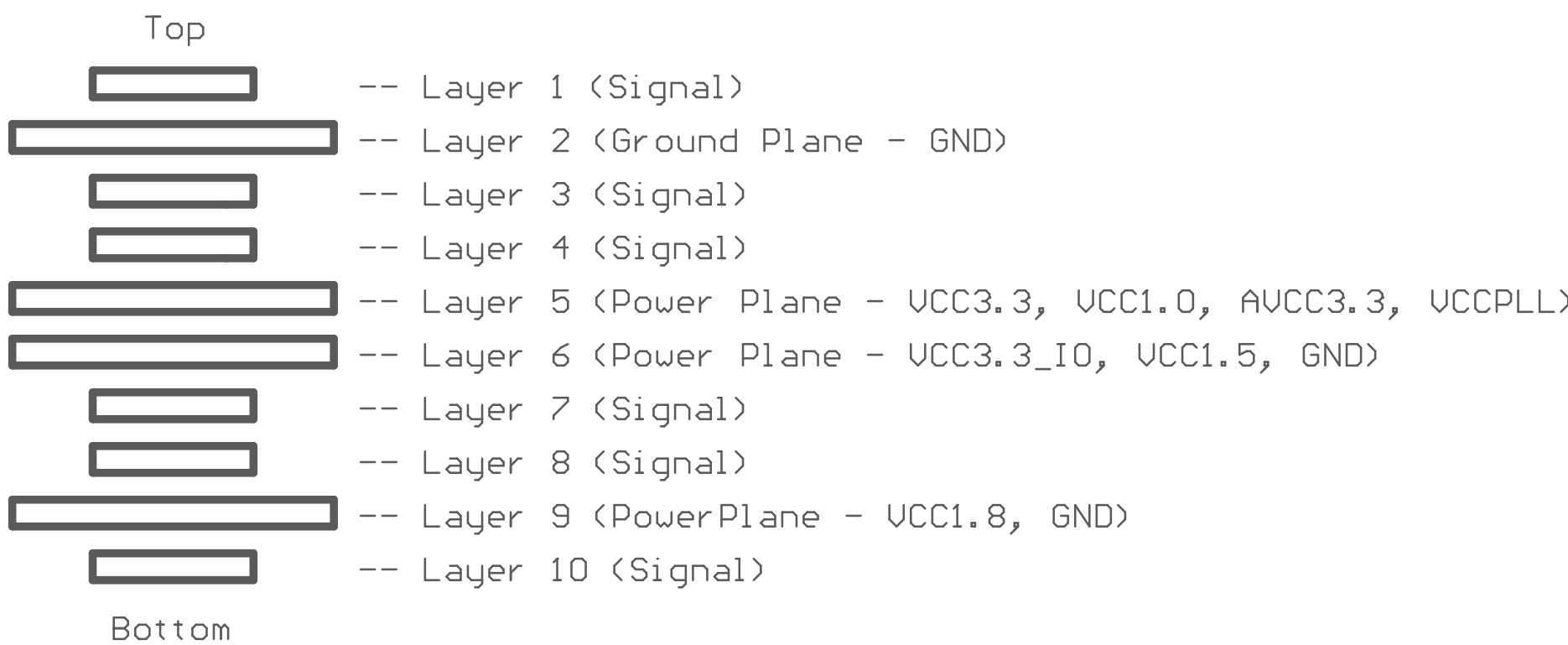
Top Overlay (Ink)



Specifications:

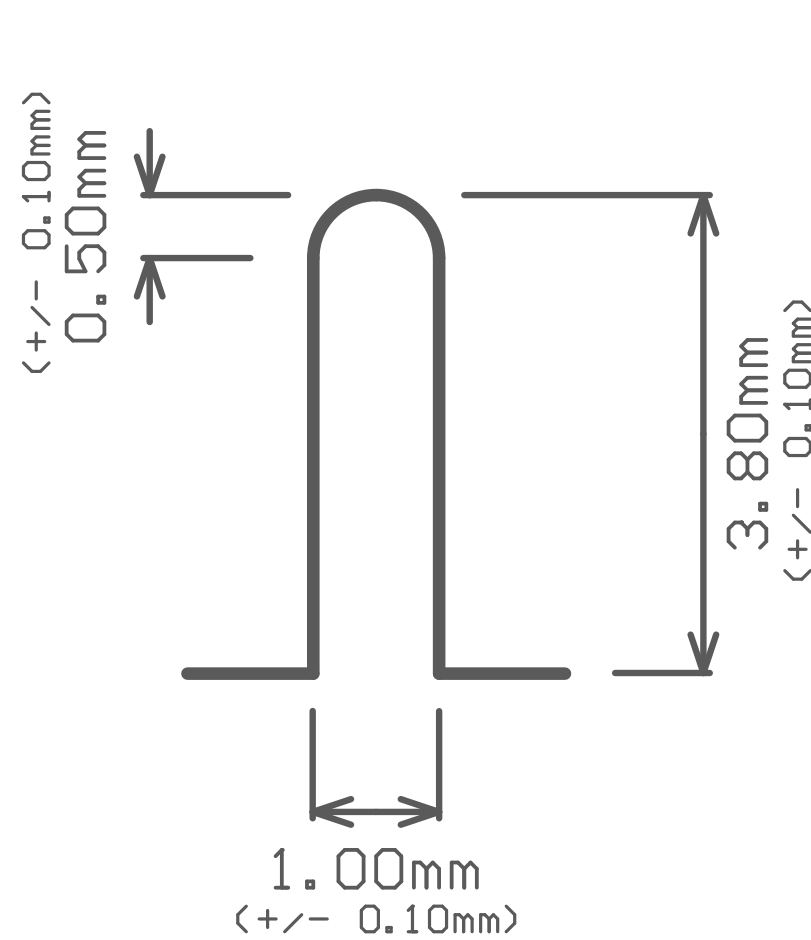
- Dielectric material is Tetrafunctional FR-4 with $T_g > 170^\circ\text{C}$
- Overall thickness is 1.0mm $\pm 0.10\text{mm}$
- Board dimensions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
- Panelization
 - Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - Panels should contain fiducial marks for X,Y alignment
- Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
- All layers use 1/2 oz. copper (before plating)
- Holes:
 - Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - Drills are plated-through holes and their locations are given in a separate drill file.
- Finish:
 - Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - Overall board finish is immersion gold.
- Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
- Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimageable, with maximum thickness of 3 mils
- Layers 2, 5, 6 and 9 are power planes and are INVERTED
- Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
- Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
- Combination of bow and twist shall not exceed 10 mils/inch along any direction
- Design origin is at the bottom-left corner of the PCB
- Testing:
 - All layers to undergo optical inspection (machine-based) of all layers before lamination
 - Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
- Locations in IPC-D-356A file are given in 2.4 English units
- South edge-to-edge connector details:
 - Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup

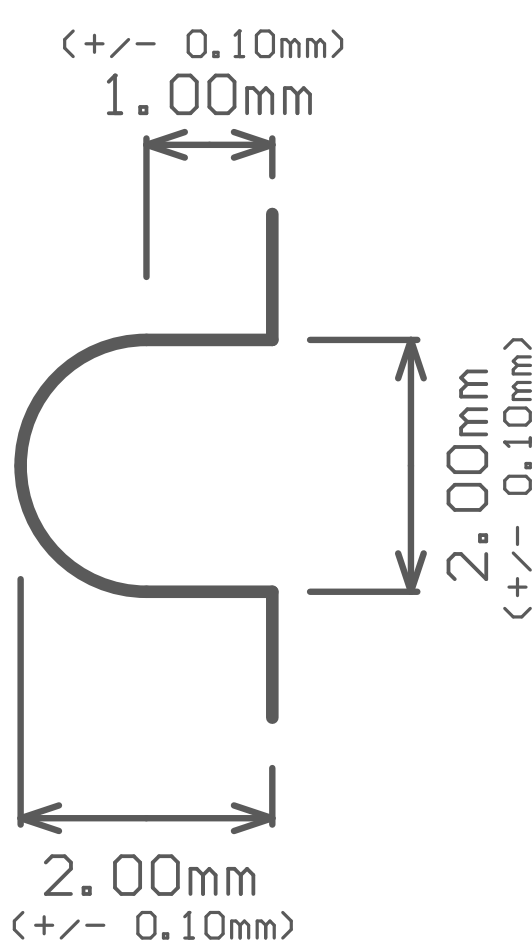


Univ. of Wisconsin—Madison Madison, WI 53706	ENGINEER: Vicente, M.		TITLE: ZYNQ—IPMC		
	PCB DESIGNER: Vicente, M.				
	DATE: 06JUN2019		PART NO.:		REV: revB1
	FILE NAME: ZYNQ_IPMC.PCBDOC		DWG NO:		SCALE: 1:1

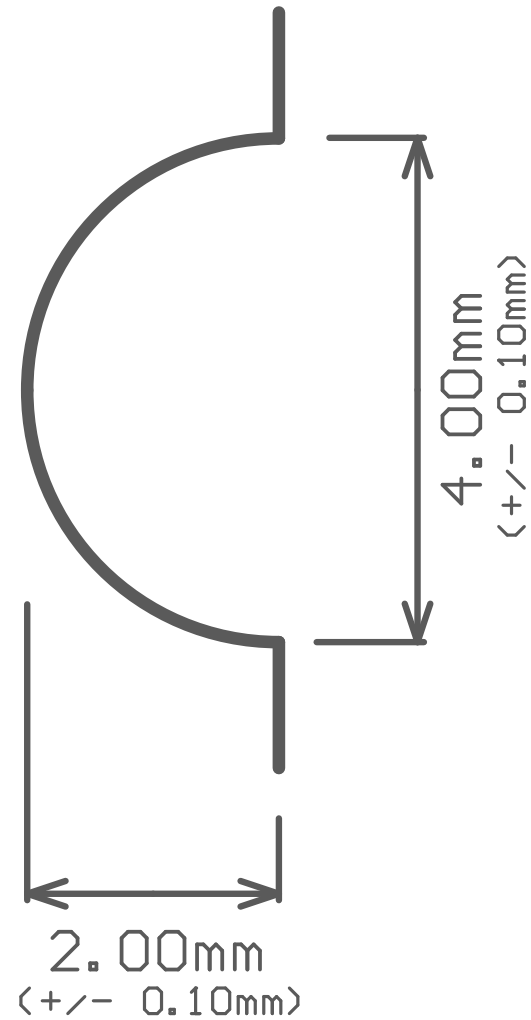
A



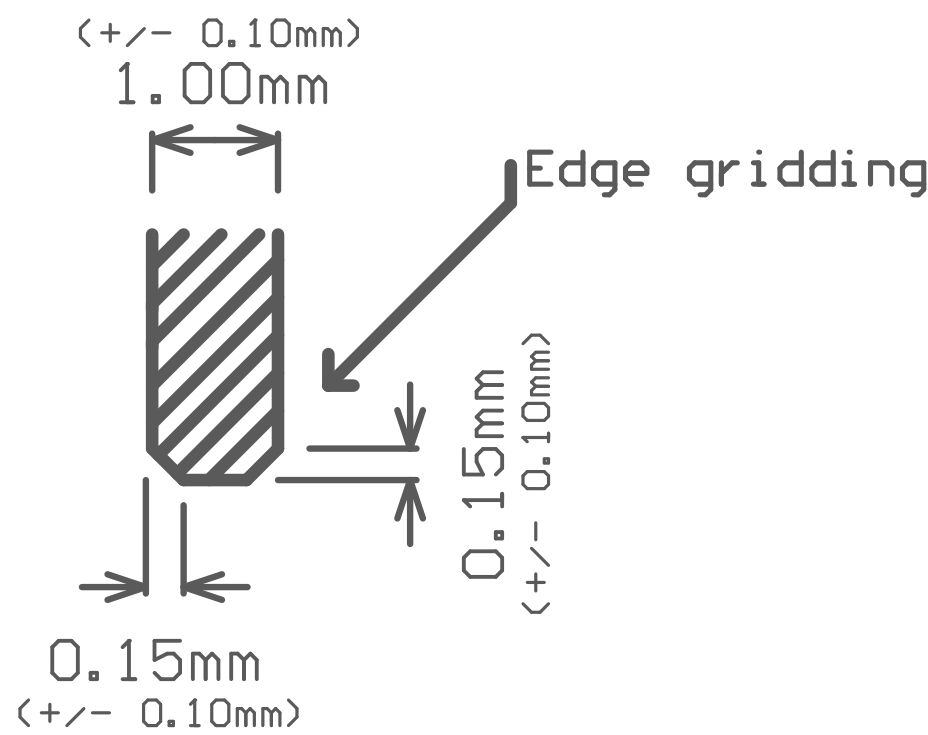
Detail 1



Detail 2



Detail 3

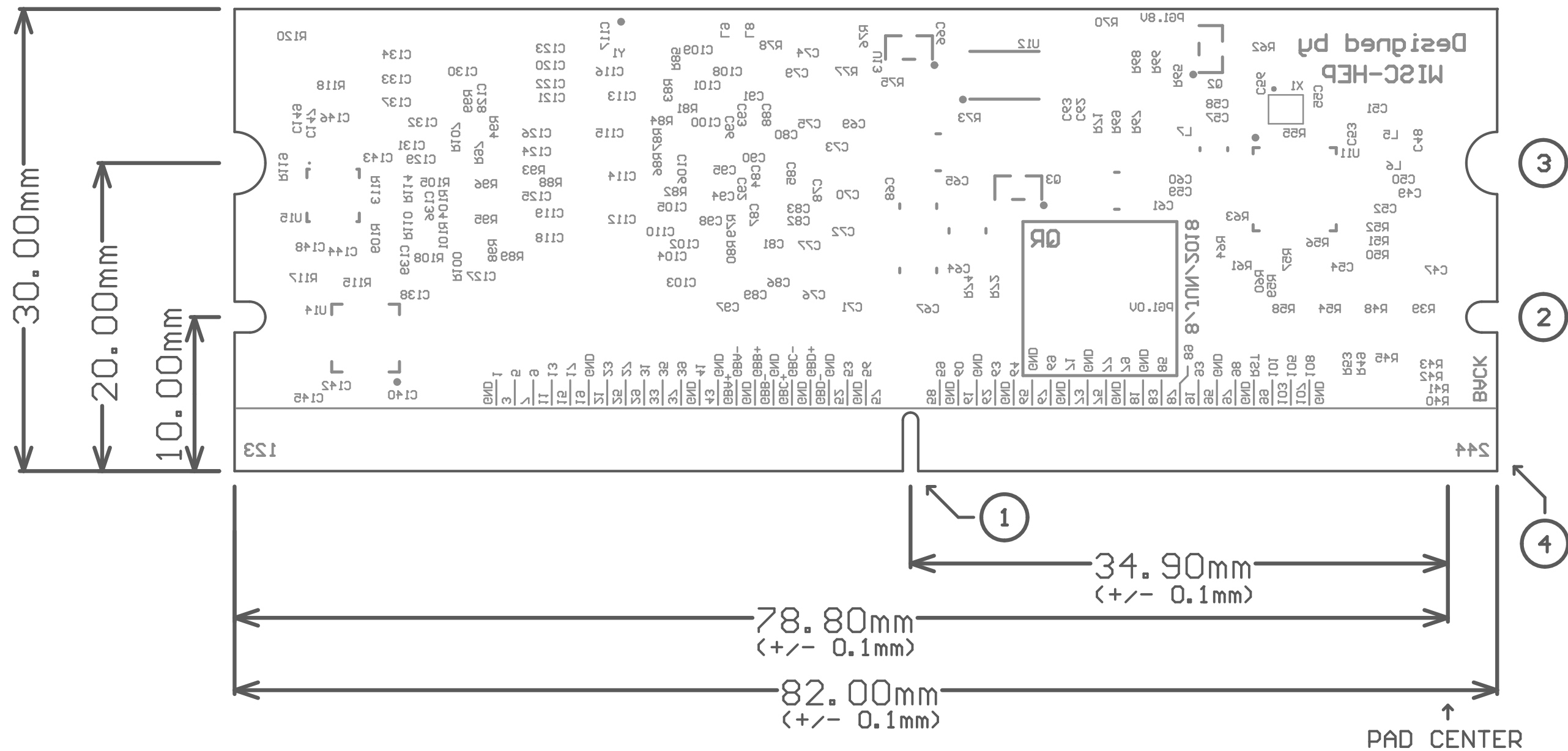


Detail 4
(PCB side view)

B

UW-IPMC MEZZANINE (revB)

Bottom Overlay (Ink)



C

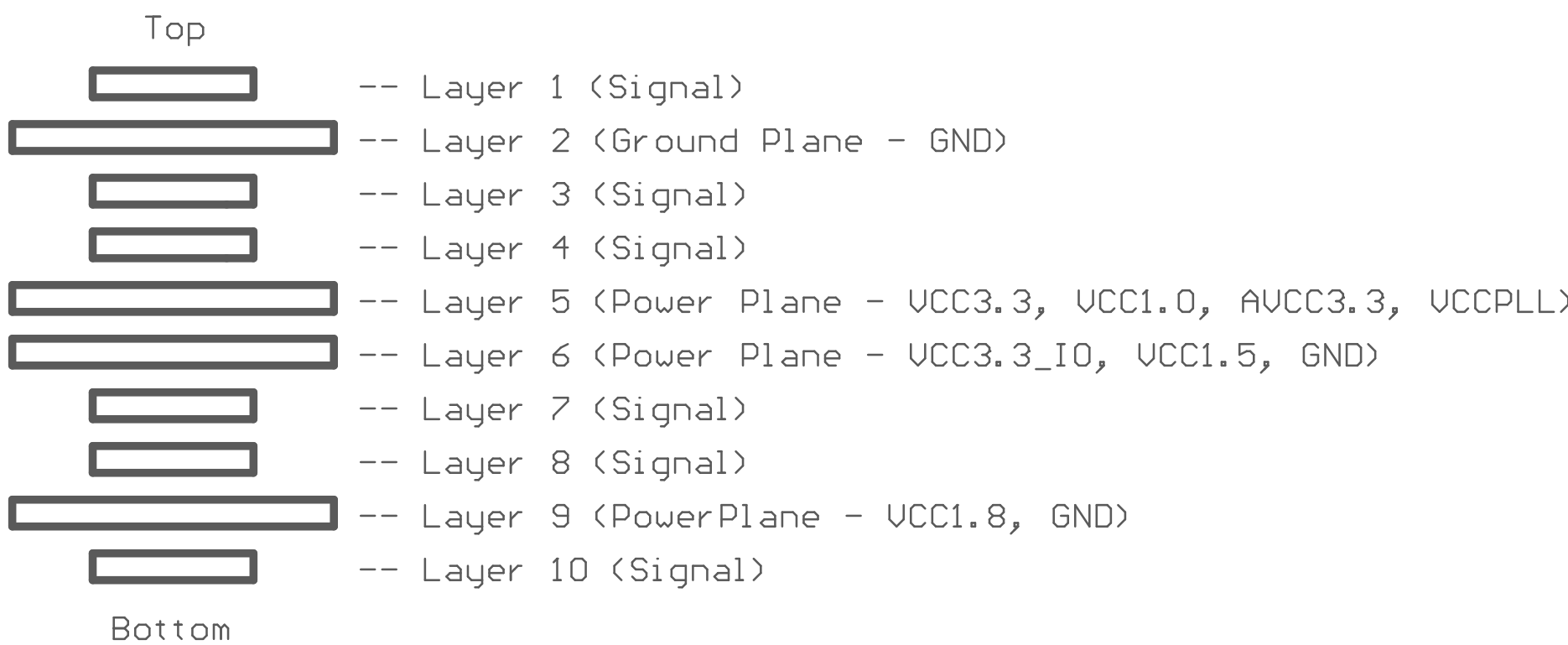
Specifications:

- Dielectric material is Tetrafunctional FR-4 with $T_g > 170^\circ\text{C}$
- Overall thickness is 1.0mm $\pm 0.10\text{mm}$
- Board dimensions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
- Panelization
 - Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - Panels should contain fiducial marks for X,Y alignment
- Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
- All layers use 1/2 oz. copper (before plating)
- Holes:
 - Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - Drills are plated-through holes and their locations are given in a separate drill file.
- Finish:
 - Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - Overall board finish is immersion gold.
- Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
- Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimable, with maximum thickness of 3 mils
- Layers 2, 5, 6 and 9 are power planes and are INVERTED
- Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
- Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
- Combination of bow and twist shall not exceed 10 mils/inch along any direction
- Design origin is at the bottom-left corner of the PCB
- Testing:
 - All layers to undergo optical inspection (machine-based) of all layers before lamination
 - Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
- Locations in IPC-D-356A file are given in 2.4 English units
- South edge-to-edge connector details:
 - Details present in page 2 of the Molex 87783-0301 datasheet (included).

A

B

Layer Stackup



D

Univ. of Wisconsin—Madison Madison, WI 53706	ENGINEER: Vicente, M.	TITLE: ZYNQ—IPMC	
	PCB DESIGNER: Vicente, M.		
	DATE: 06JUN2019	PART NO.:	REV: revB1
	FILE NAME: ZYNQ_IPMC.PCBDOC	DWG NO:	SCALE: 1:1

D

A

B

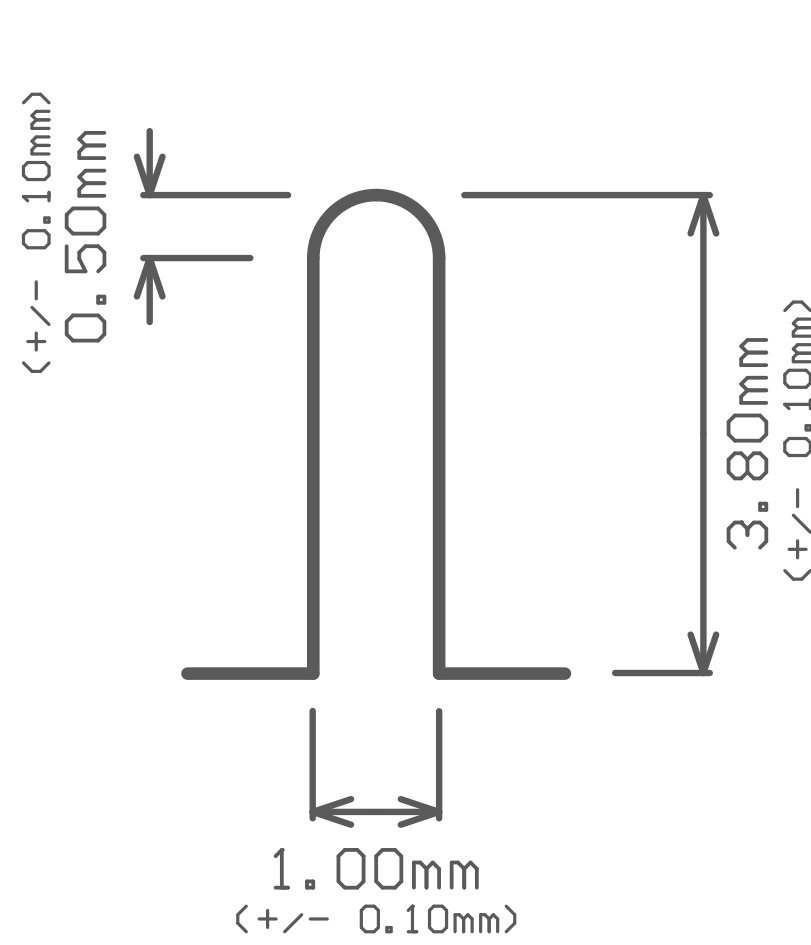
C

D

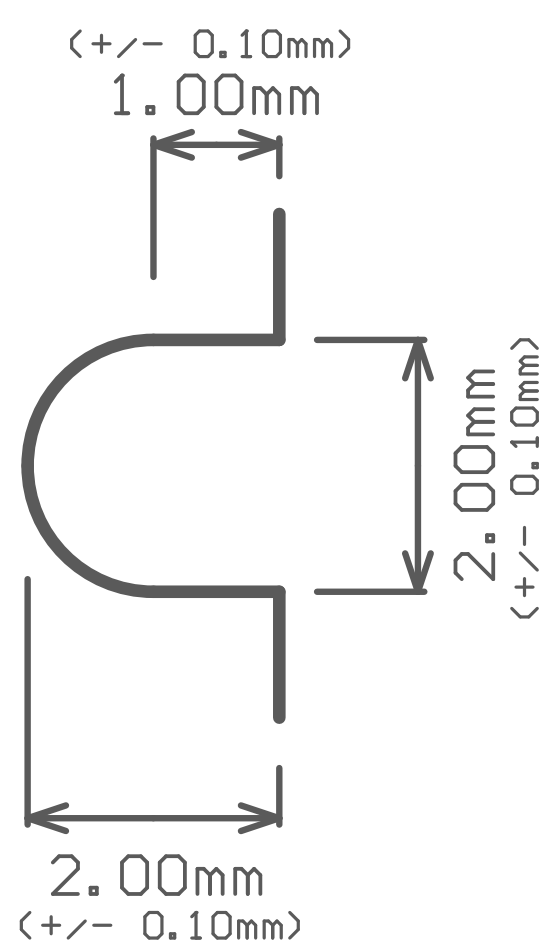
A

B

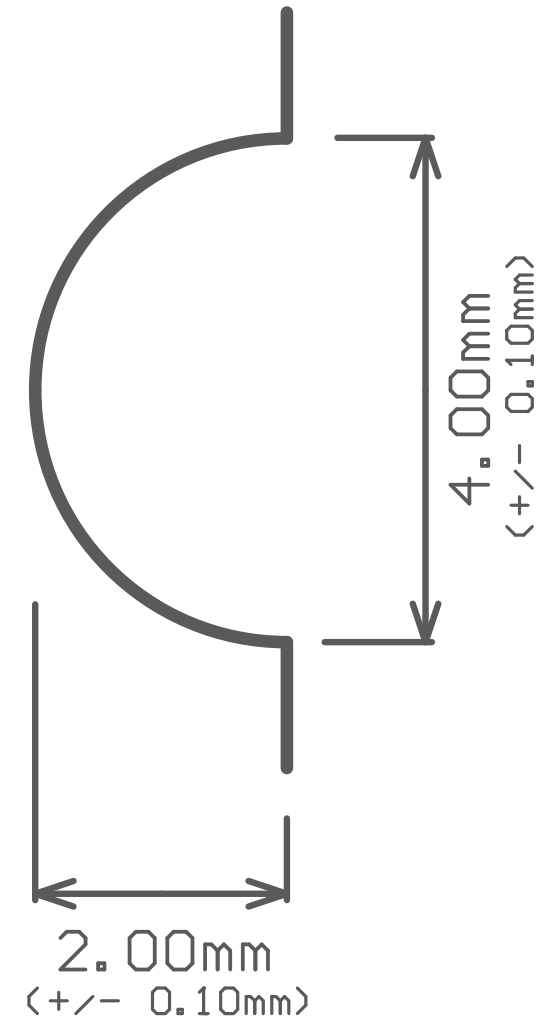
D



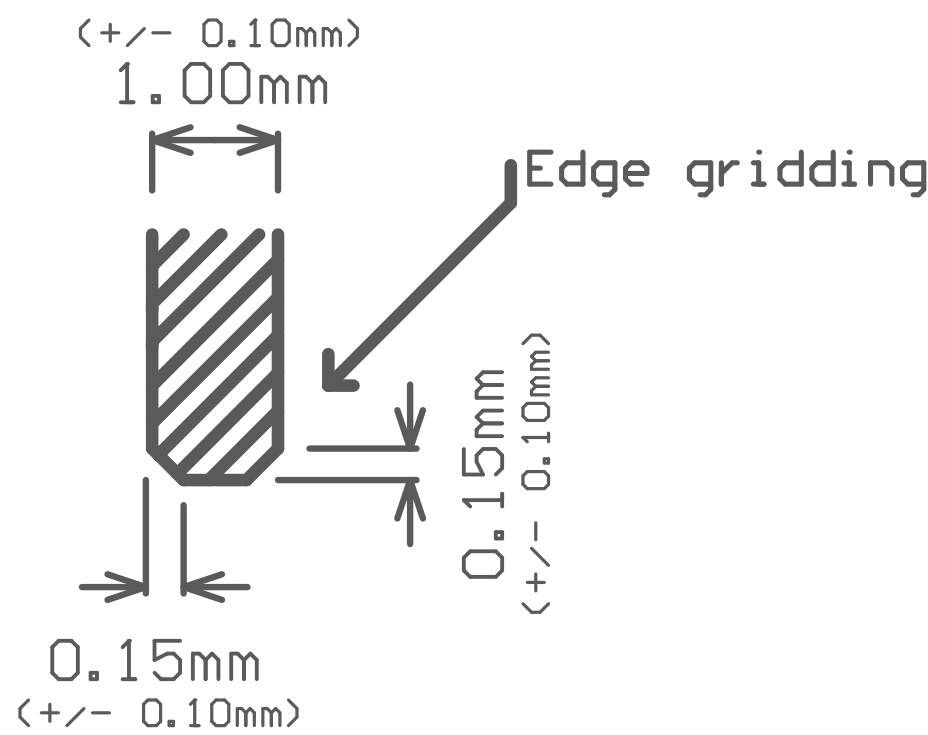
Detail 1



Detail 2



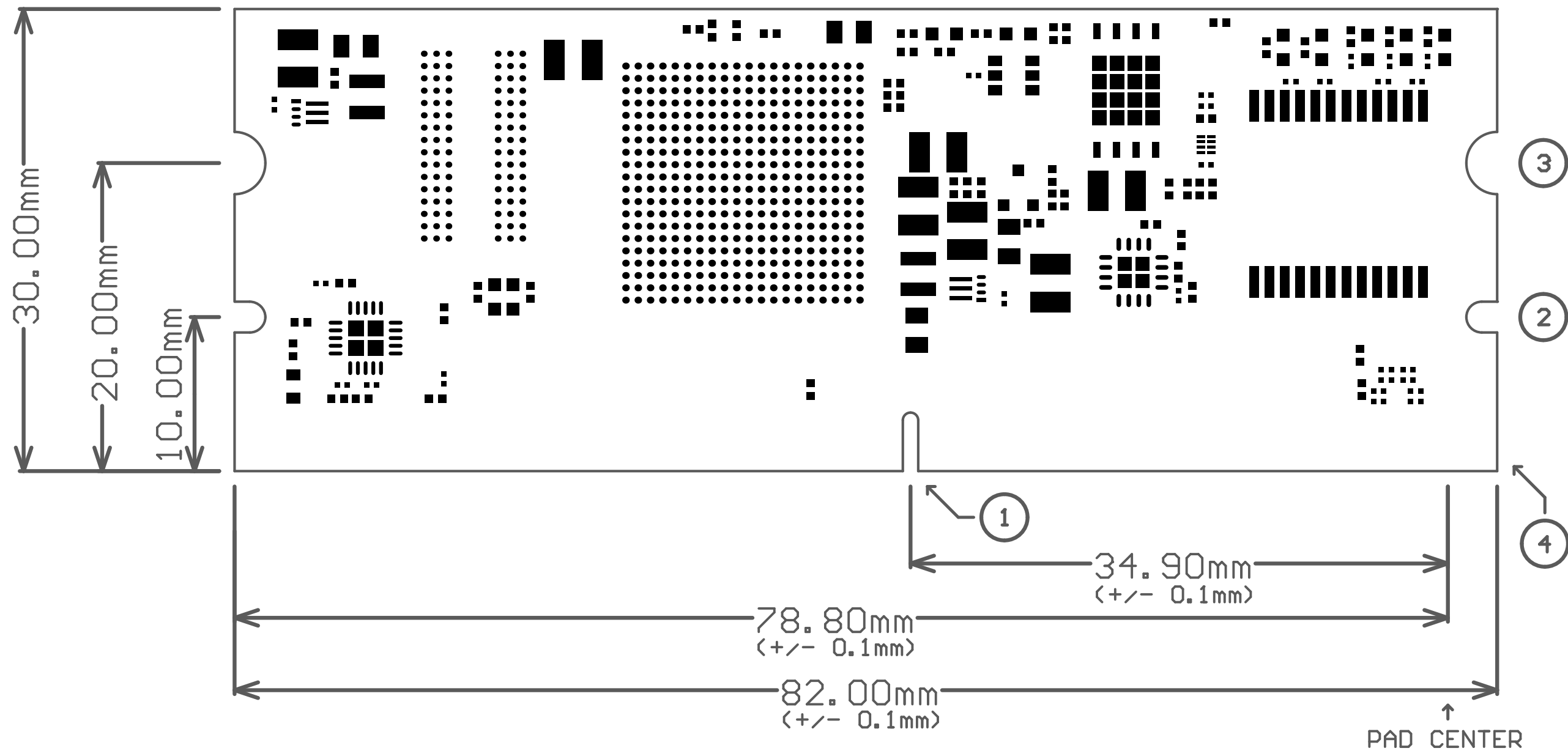
Detail 3



Detail 4
(PCB side view)

UW-IPMC MEZZANINE (revB)

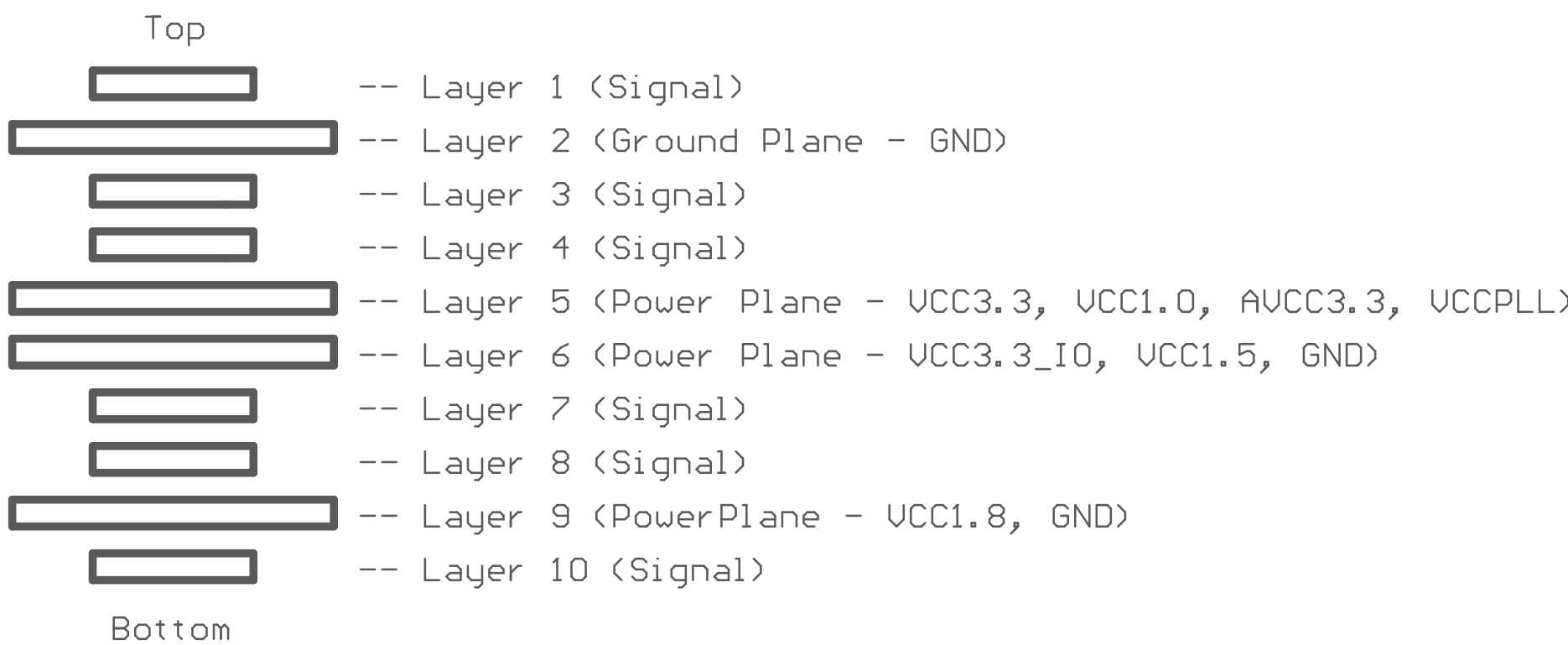
Top Paste (Paste)



Specifications:

- Dielectric material is Tetrafunctional FR-4 with $T_g > 170\text{ }^{\circ}\text{C}$
- Overall thickness is 1.0mm $\pm 0.10\text{mm}$
- Board dimentions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
- Panelization
 - Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - Panels should contain fiducial marks for X,Y alignment
- Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
- All layers use 1/2 oz. copper (before plating)
- Holes:
 - Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - Drills are plated-through holes and their locations are given in a separate drill file.
- Finish:
 - Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - Overall board finish is immersion gold.
- Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
- Red colored solder mask shall be applied to both top and bottom surfaces.
Mask shall be photoimagable, with maximum thickness of 3 mils
- Layers 2, 5, 6 and 9 are power planes and are INVERTED
- Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
- Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
- Combination of bow and twist shall not exceed 10 mils/inch along any direction
- Design origin is at the bottom-left corner of the PCB
- Testing:
 - All layers to undergo optical inspection (machine-based) of all layers before lamination
 - Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
- Locations in IPC-D-356A file are given in 2.4 English units
- South edge-to-edge connector details:
 - Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup



Univ. of Wisconsin—Madison Madison, WI 53706	ENGINEER: Vicente, M.	TITLE: ZYNQ—IPMC	
	PCB DESIGNER: Vicente, M.		
	DATE: 06JUN2019	PART NO.:	REV: revB1
	FILE NAME: ZYNQ_IPMC.PCBDOC	DWG NO:	SCALE: 1:1

Technical drawing of a U-shaped component. The dimensions are:

- Width: 1.00mm (+/- 0.10mm)
- Height: 3.80mm (+/- 0.10mm)
- Top Radius: 0.50mm (+/- 0.10mm)

Detail 1

Technical drawing of a U-shaped component. The drawing shows the component with the following dimensions:

- Top horizontal width: 1.00mm ($\pm 0.10\text{mm}$)
- Right vertical height: 2.00mm ($\pm 0.10\text{mm}$)
- Bottom horizontal width: 2.00mm ($\pm 0.10\text{mm}$)

Detail 2

Technical drawing of a semi-circular profile. The horizontal width is dimensioned as 2.00mm (+/- 0.10mm). The vertical height is dimensioned as 4.00mm (+/- 0.10mm).

Detail 3

Technical drawing of a specimen with the following dimensions and labels:

- Top width: $(+/- 0.10\text{mm})$
- Top width: 1.00mm
- Right side label: Edge gridding
- Right side height: 0.15mm
- Right side height: $(+/- 0.10\text{mm})$
- Bottom width: 0.15mm
- Bottom width: $(+/- 0.10\text{mm})$

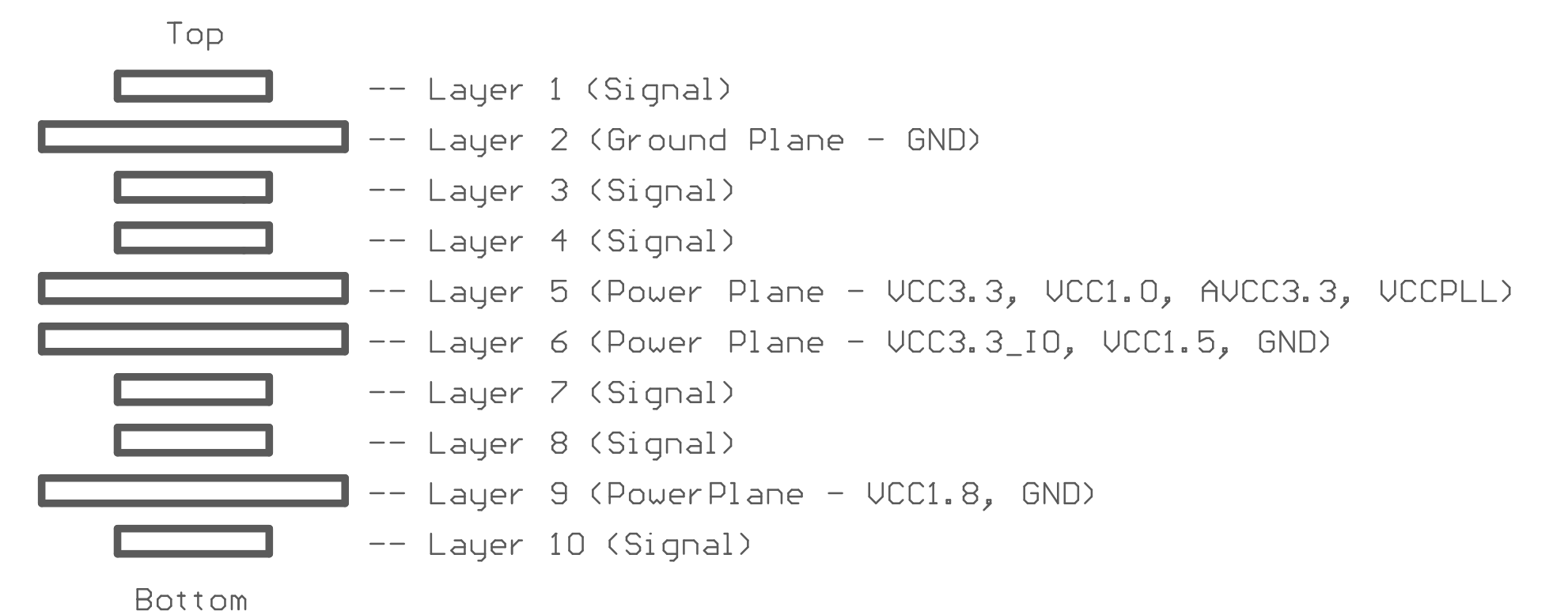
Detail 4

(PCB side view)

Specifications:

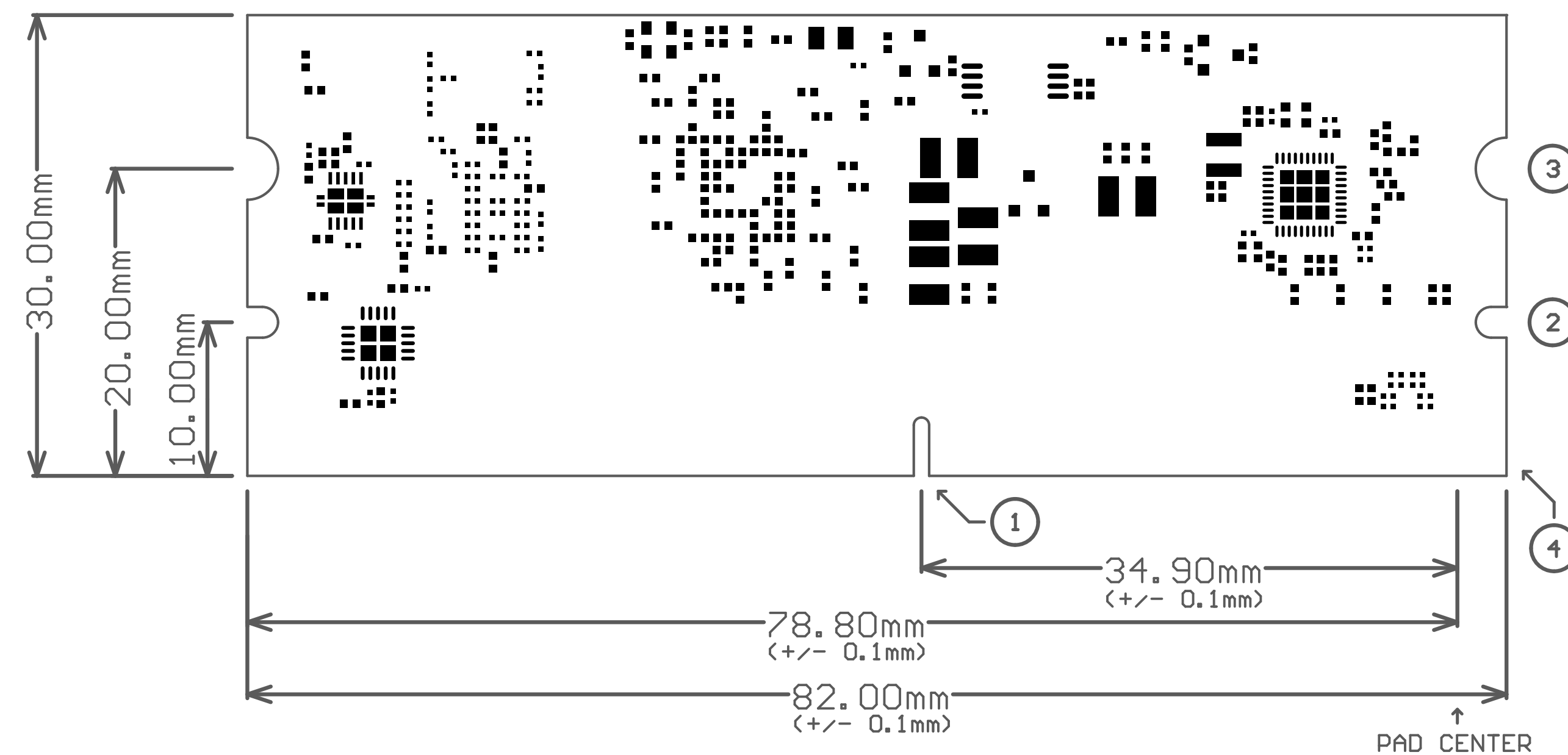
1. Dielectric material is Tetrafunctional FR-4 with Tg > 170 C
2. Overall thickness is 1.0mm +/- 0.10mm
3. Board dimensions are 82 by 30mm with tolerances of +/- 0.15mm unless specified in drawing.
4. Panelization
 - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - b. Panels should contain fiducial marks for X,Y alignment
5. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
 40 Ohm: 6 mil tracks in artwork
 50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
 40 Ohm: 9.5 mil tracks in artwork
 50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
6. All layers use 1/2 oz. copper (before plating)
7. Holes:
 - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - d. Drills are plated-through holes and their locations are given in a separate drill file.
8. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface.
 Area to receive hard gold finish is identified in two separate photoplot layers.
 Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
9. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
10. Red colored solder mask shall be applied to both top and bottom surfaces.
 Mask shall be photoimagable, with maximum thickness of 3 mils
11. Layers 2, 5, 6 and 9 are power planes and are INVERTED
12. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
 DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing.
 Testing report to be enclosed with the quality control documentation shipped with the boards.
17. Locations in IPC-D-356A file are given in 2.4 English units
18. South edge-to-edge connector details:
 - a. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup



UW-IPMC MEZZANINE (revB)

Bottom Paste (Paste)



Univ. of Wisconsin—Madison
Madison, WI 53706

ENGINEER:
Vicente, M.

PCB DESIGNER:
Vicente, M.

DATE:
06JUN2019

FILE NAME:
ZYNQ_IPMC.PCBDOC

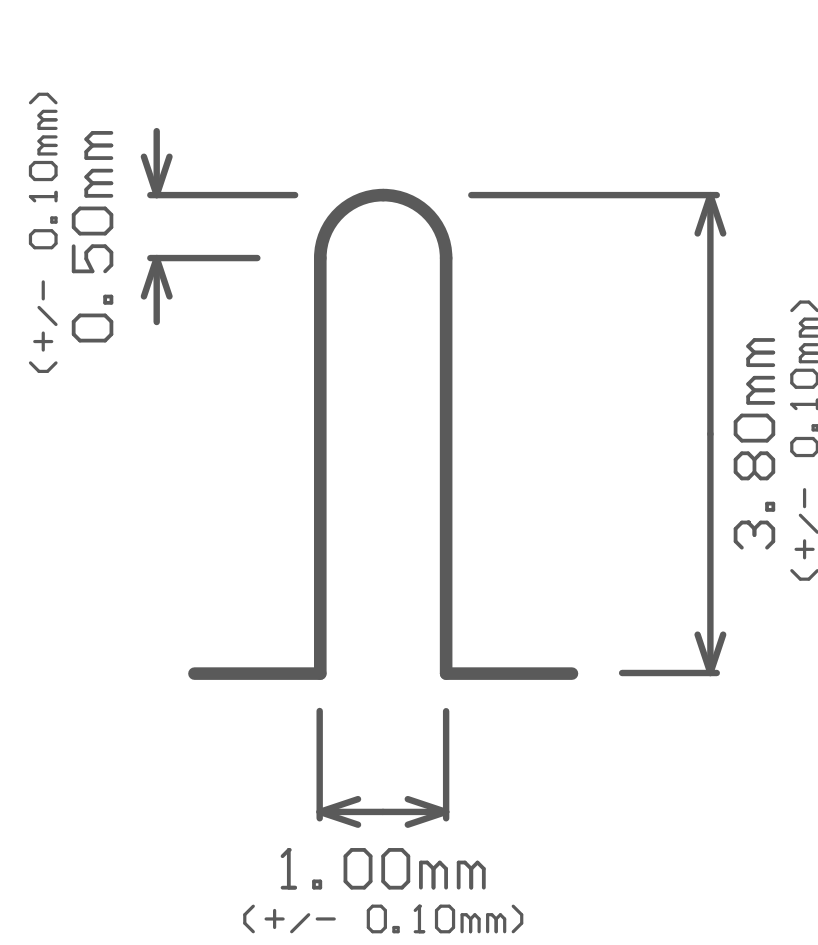
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ZYNQ-IPMC

PART NO.:

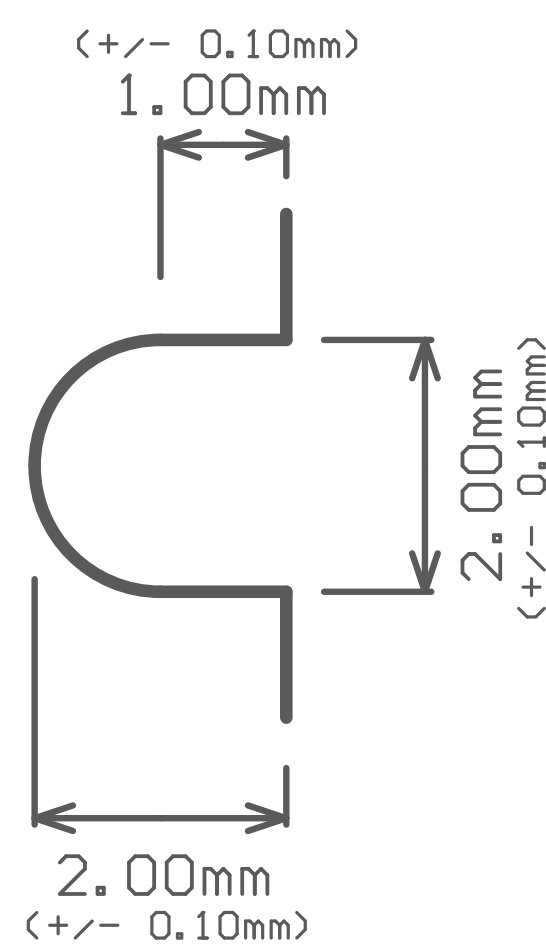
REV:
revB1

SCALE:
1:1

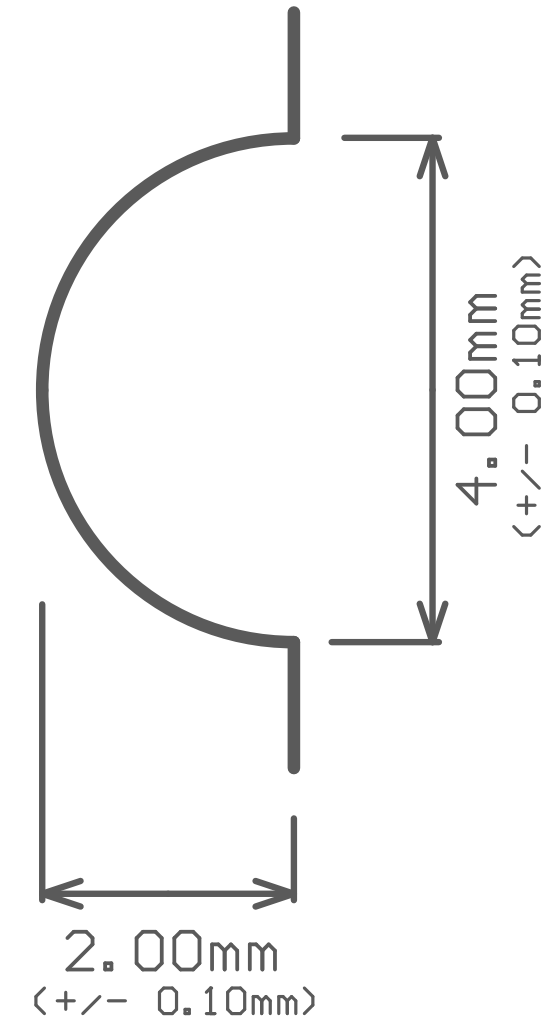
A



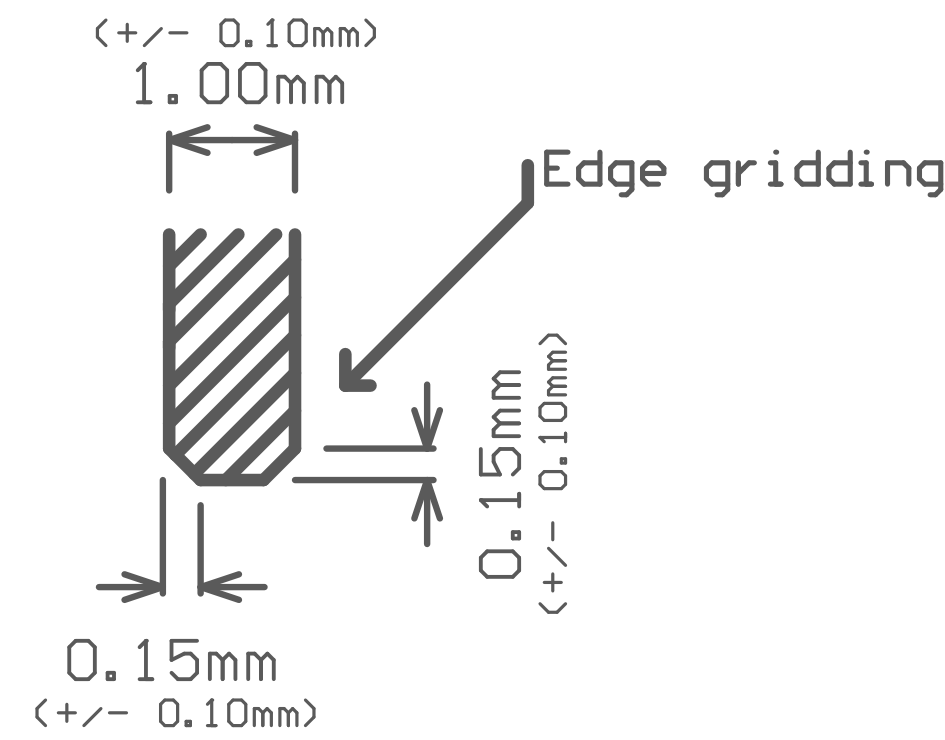
Detail 1



Detail 2



Detail 3

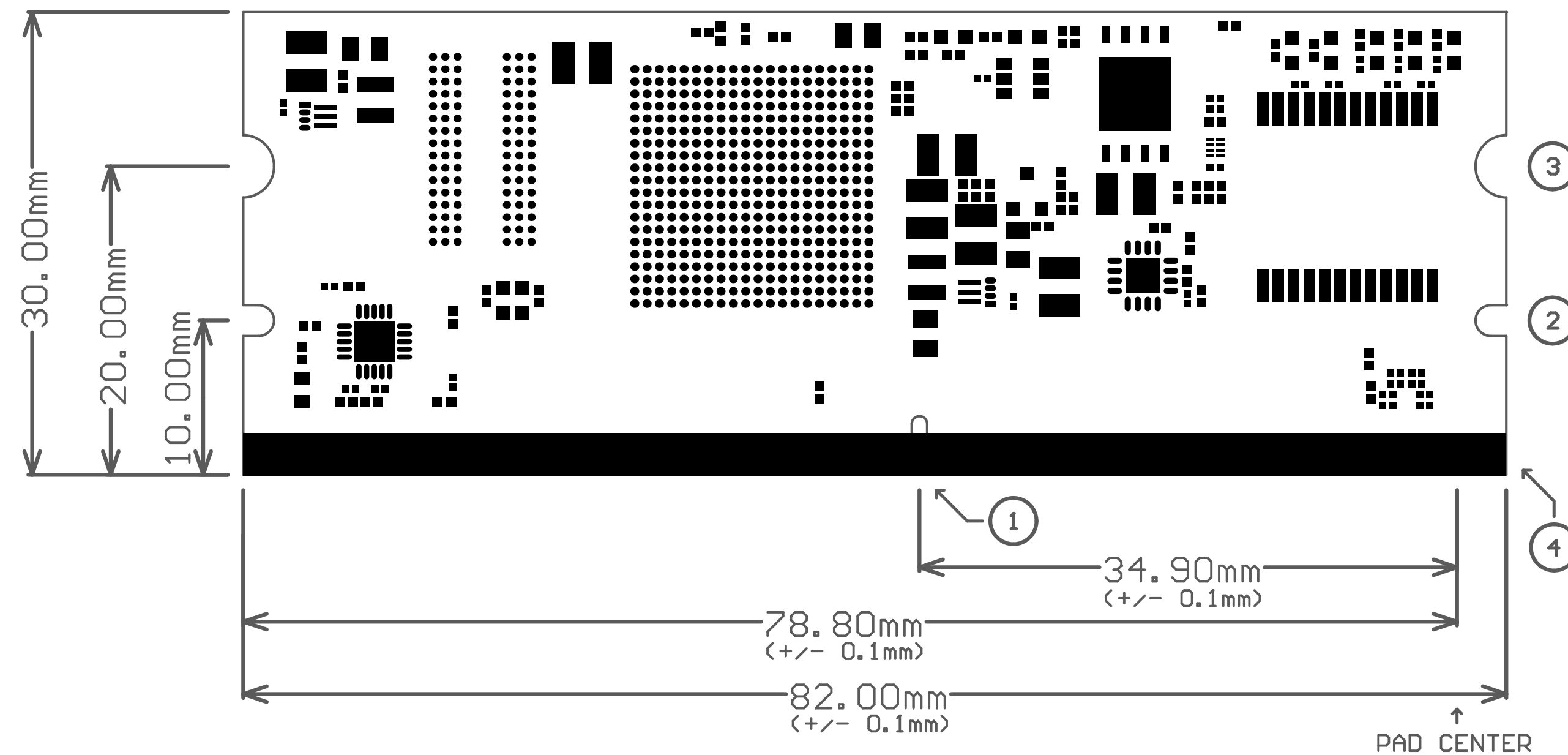


Detail 4
(PCB side view)

B

UW-IPMC MEZZANINE (revB)

Top Solder (Mask)



C

Specifications:

- Dielectric material is Tetrafunctional FR-4 with $T_g > 170\text{ }^{\circ}\text{C}$
- Overall thickness is 1.0mm $\pm 0.10\text{mm}$
- Board dimensions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
- Panelization
 - Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - Panels should contain fiducial marks for X,Y alignment
- Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
- All layers use 1/2 oz. copper (before plating)
- Holes:
 - Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - Drills are plated-through holes and their locations are given in a separate drill file.
- Finish:
 - Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - Overall board finish is immersion gold.
- Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
- Red colored solder mask shall be applied to both top and bottom surfaces.
Mask shall be photomailable, with maximum thickness of 3 mils
- Layers 2, 5, 6 and 9 are power planes and are INVERTED
- Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
- Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
- Combination of bow and twist shall not exceed 10 mils/inch along any direction
- Design origin is at the bottom-left corner of the PCB
- Testing:
 - All layers to undergo optical inspection (machine-based) of all layers before lamination
 - Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
DC resistance shall be 10 ohms or less
 - Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
- Locations in IPC-D-356A file are given in 2.4 English units
- South edge-to-edge connector details:
 - Details present in page 2 of the Molex 87783-0301 datasheet (included).

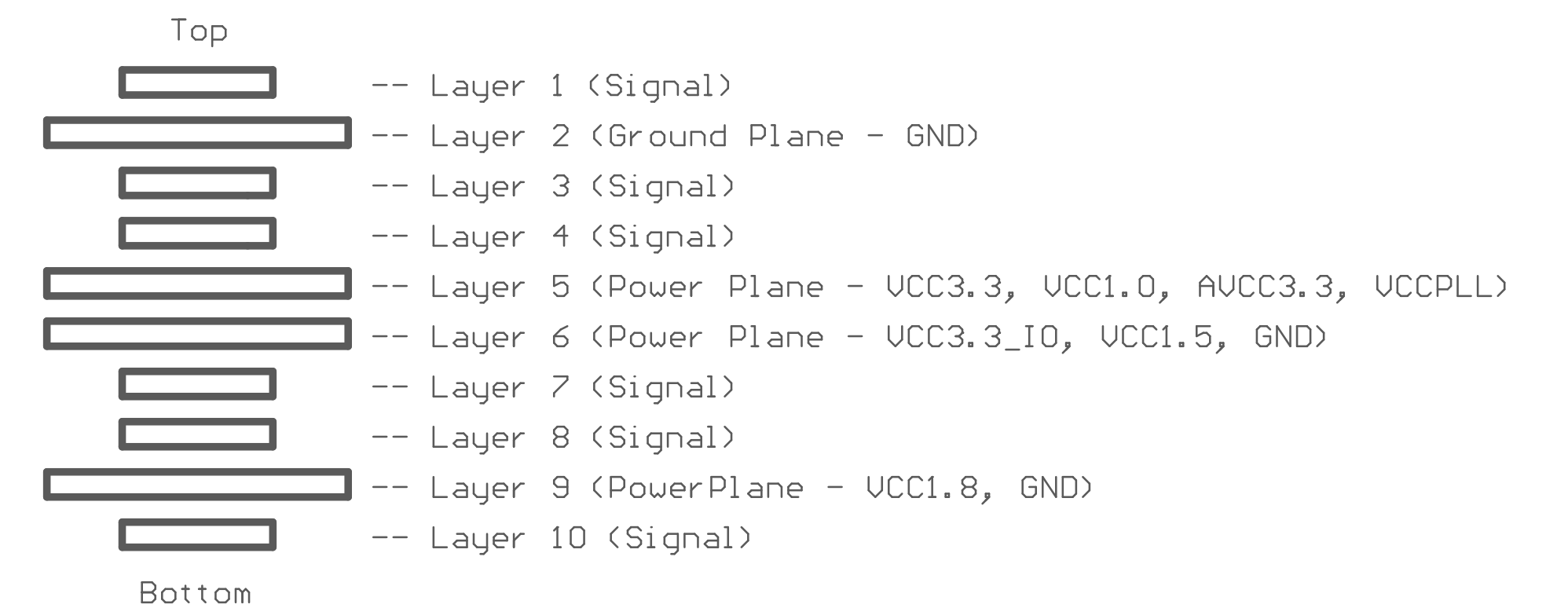
A

B

D

D

Layer Stackup



Univ. of Wisconsin—Madison Madison, WI 53706	ENGINEER: Vicente, M.	TITLE: ZYNQ—IPMC	
	PCB DESIGNER: Vicente, M.		
	DATE: 06JUN2019	PART NO.:	REV: revB1
	FILE NAME: ZYNQ_IPMC.PCBDOC	DWG NO:	SCALE: 1:1

A

B

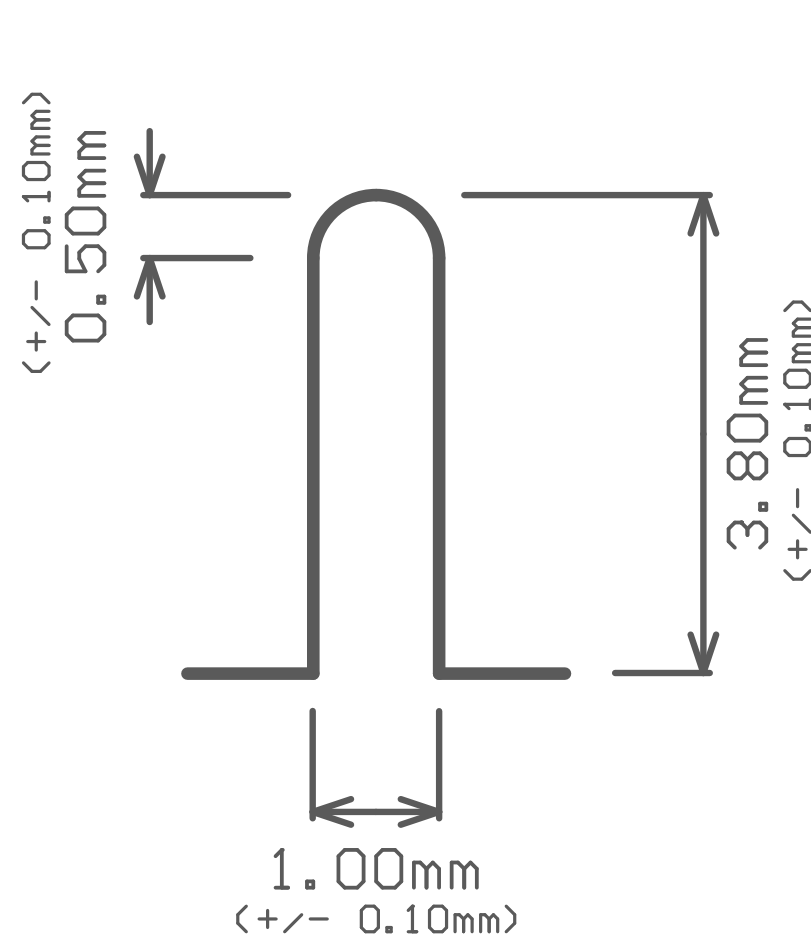
C

D

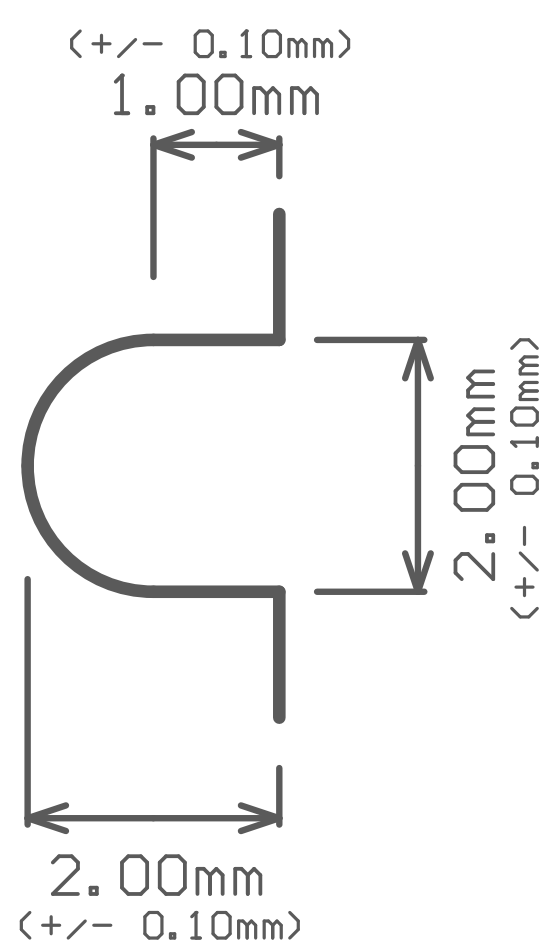
A

B

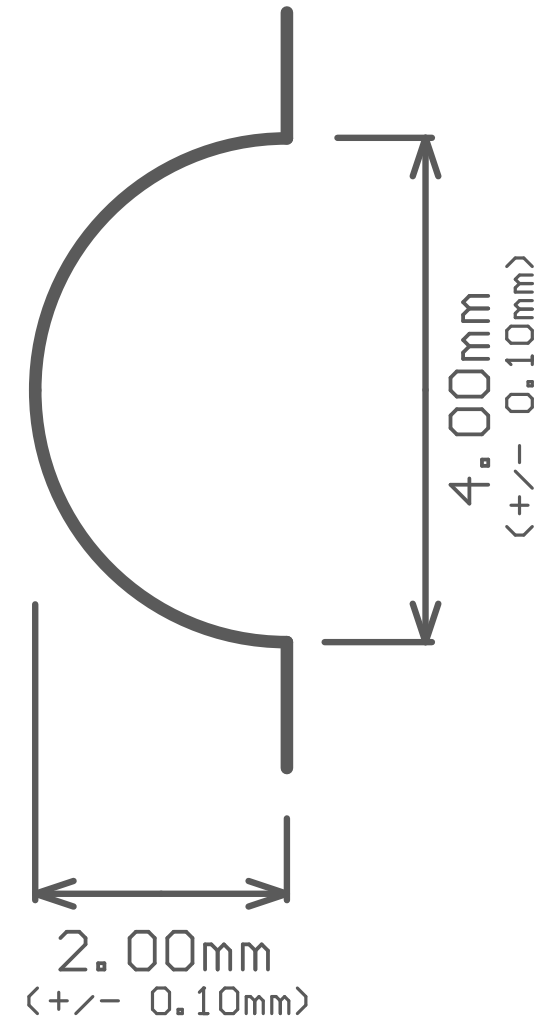
D



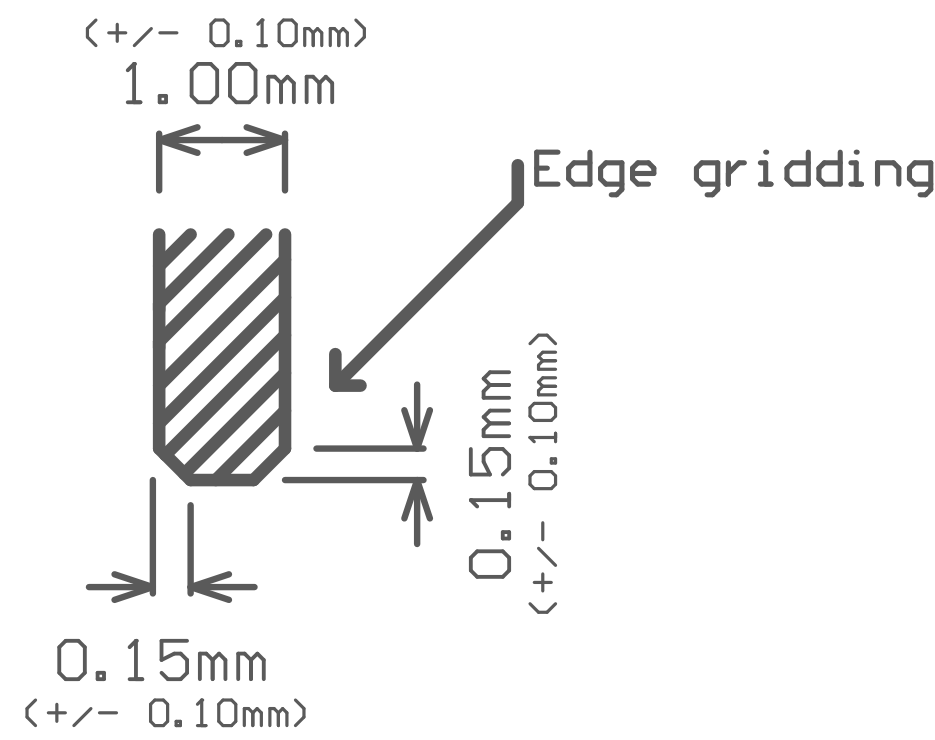
Detail 1



Detail 2



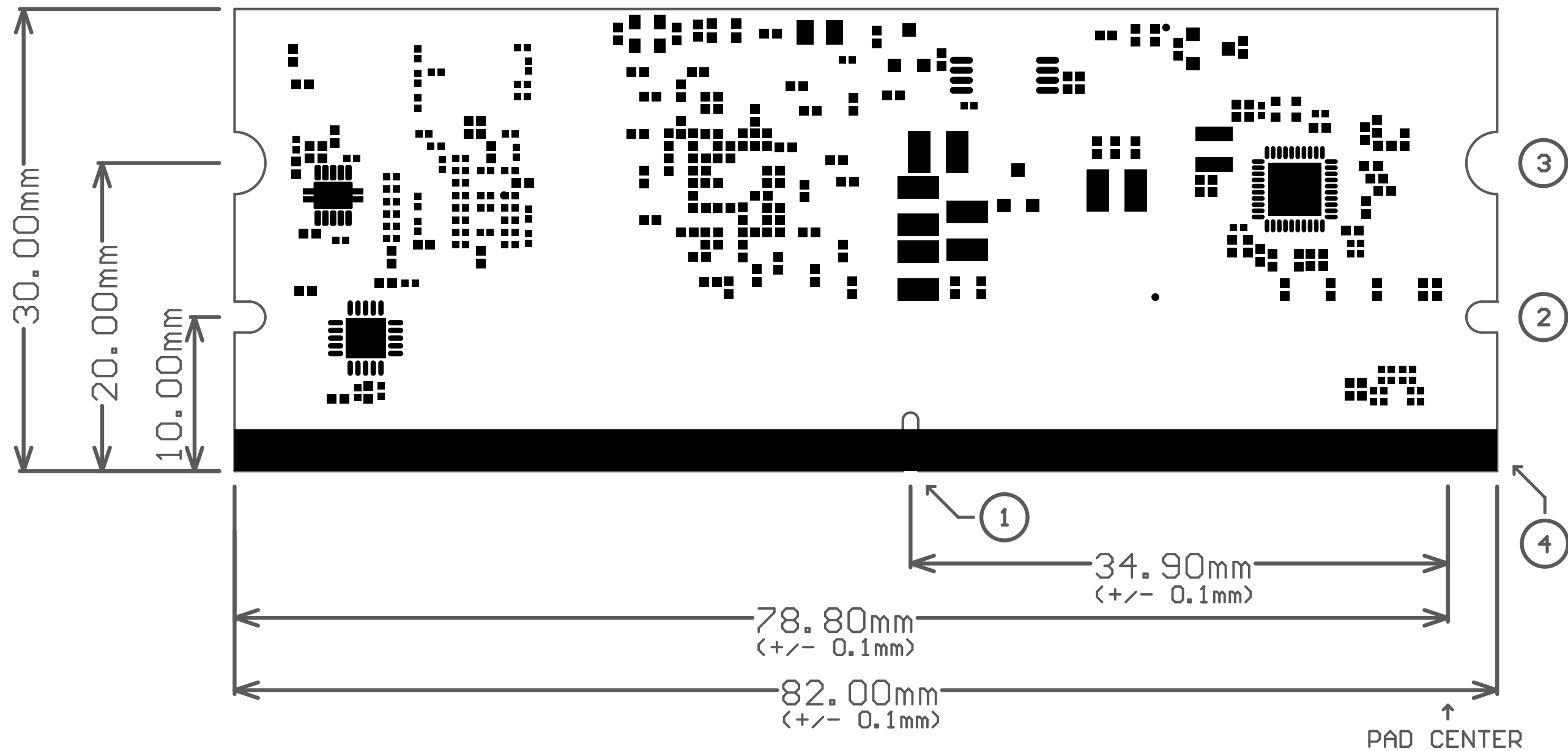
Detail 3



Detail 4
(PCB side view)

UW-IPMC MEZZANINE (revB)

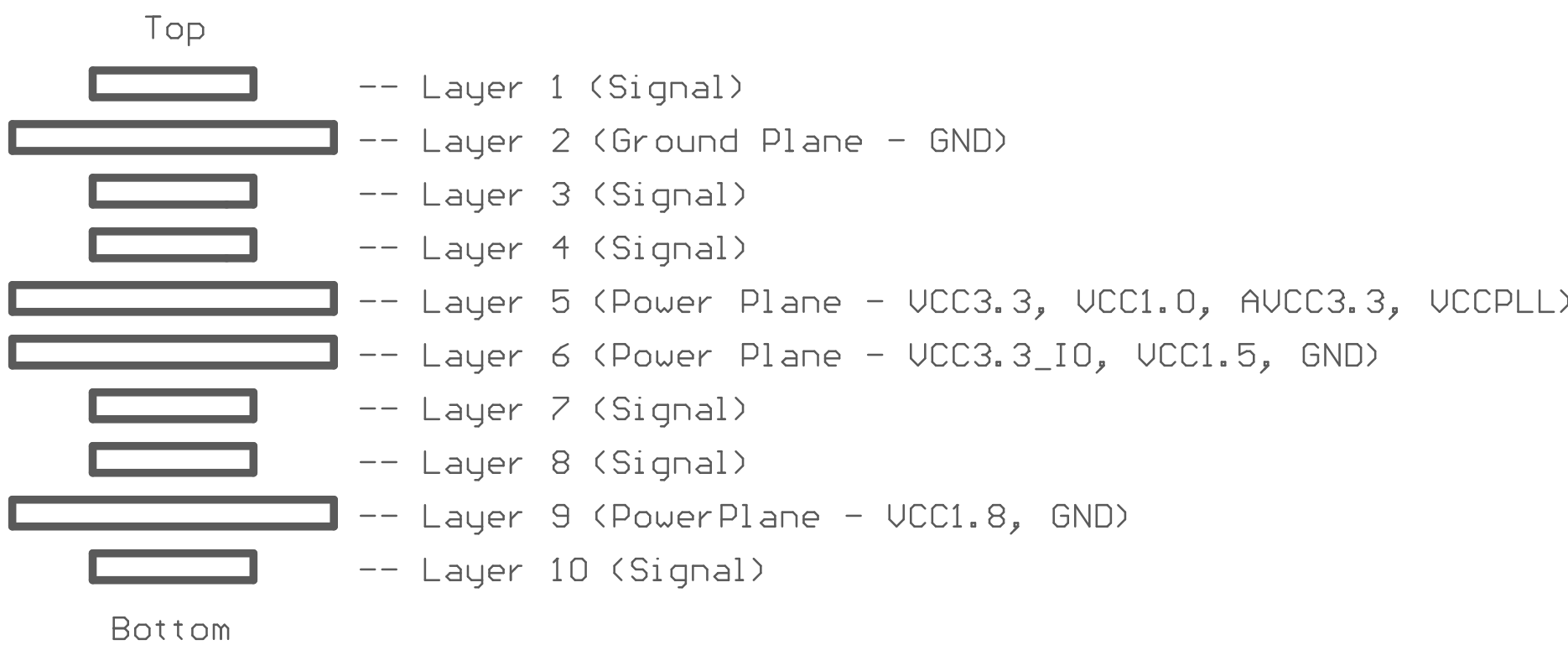
Bottom Solder (Mask)



Specifications:

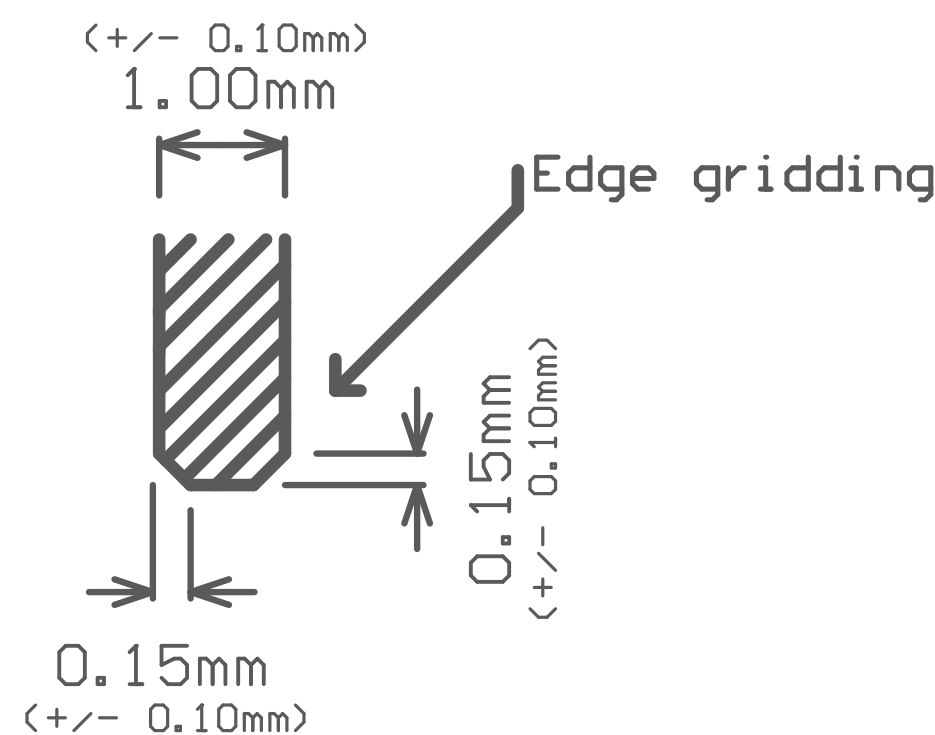
- Dielectric material is Tetrafunctional FR-4 with $T_g > 170\text{ }^{\circ}\text{C}$
- Overall thickness is 1.0mm $\pm 0.10\text{mm}$
- Board dimensions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
- Panelization
 - Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - Panels should contain fiducial marks for X,Y alignment
- Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
- All layers use 1/2 oz. copper (before plating)
- Holes:
 - Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - Drills are plated-through holes and their locations are given in a separate drill file.
- Finish:
 - Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - Overall board finish is immersion gold.
- Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
- Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimable, with maximum thickness of 3 mils
- Layers 2, 5, 6 and 9 are power planes and are INVERTED
- Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
- Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
- Combination of bow and twist shall not exceed 10 mils/inch along any direction
- Design origin is at the bottom-left corner of the PCB
- Testing:
 - All layers to undergo optical inspection (machine-based) of all layers before lamination
 - Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
- Locations in IPC-D-356A file are given in 2.4 English units
- South edge-to-edge connector details:
 - Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup



Univ. of Wisconsin—Madison Madison, WI 53706	ENGINEER: Vicente, M.	TITLE: ZYNQ—IPMC	
	PCB DESIGNER: Vicente, M.		
	DATE: 06JUN2019	PART NO.:	REV: revB1
	FILE NAME: ZYNQ_IPMC.PCBDOC	DWG NO:	SCALE: 1:1

A



Detail 4

(PCB side view)

B

Technical drawing of a rectangular component with dimensions and callouts:

- Overall height: 30.00mm
- Height of the top section: 20.00mm
- Height of the bottom section: 10.00mm
- Overall width: 82.00mm (+/- 0.1mm)
- Width of the bottom section: 34.90mm (+/- 0.1mm)
- Width of the top section: 78.80mm (+/- 0.1mm)
- Callout 1: Points to the bottom edge of the top section.
- Callout 2: Points to the top edge of the bottom section.
- Callout 3: Points to the top edge of the top section.
- Callout 4: Points to the bottom edge of the bottom section.
- Label: PAD CENTER with an arrow pointing to the center of the bottom edge.

C

D

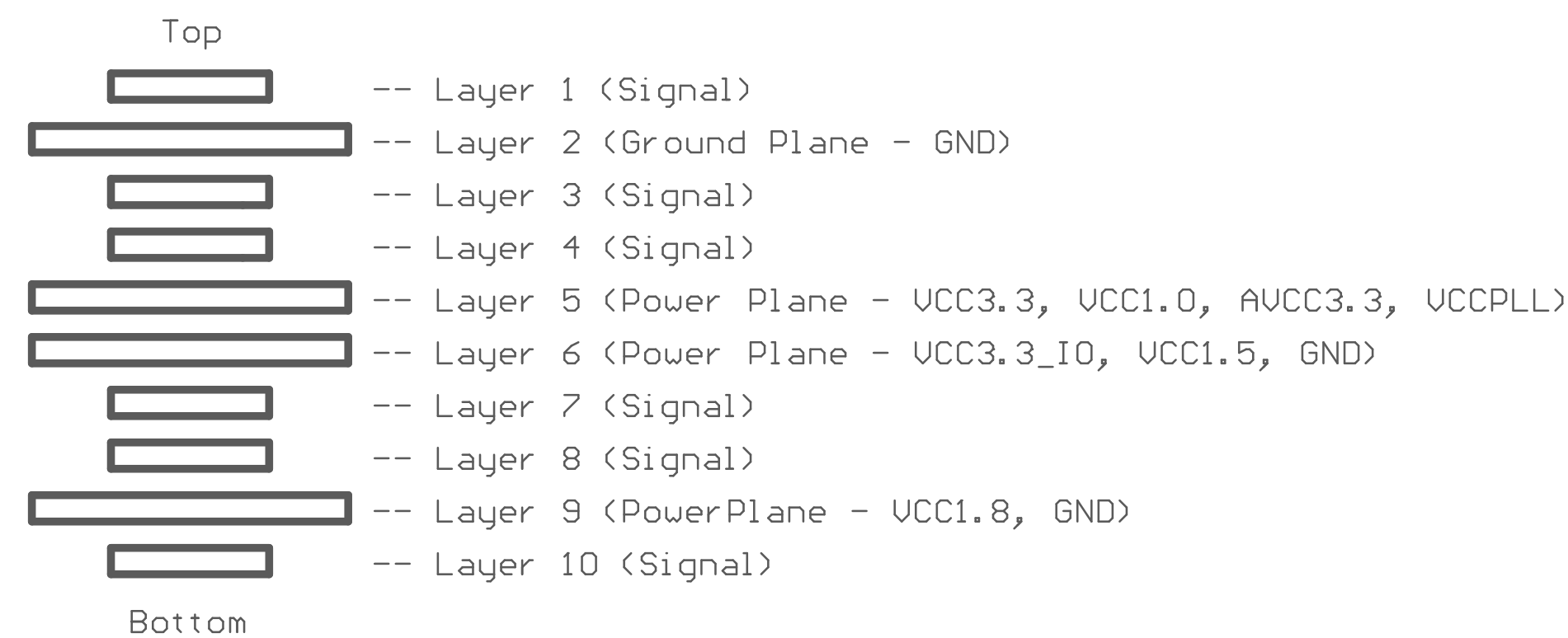
Specifications:

1. Dielectric material is Tetrafunctional FR-4 with Tg > 170 C
2. Overall thickness is 1.0mm +/- 0.10mm
3. Board dimensions are 82 by 30mm with tolerances of +/- 0.15mm unless specified in drawing.
4. Panelization
 - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - b. Panels should contain fiducial marks for X,Y alignment
5. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
 40 Ohm: 6 mil tracks in artwork
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 50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
6. All layers use 1/2 oz. copper (before plating)
7. Holes:
 - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - d. Drills are plated-through holes and their locations are given in a separate drill file.
8. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface.
 Area to receive hard gold finish is identified in two separate photoplot layers.
 Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
9. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
10. Red colored solder mask shall be applied to both top and bottom surfaces.
Mask shall be photoimageable, with maximum thickness of 3 mils
11. Layers 2, 5, 6 and 9 are power planes and are INVERTED
12. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
 DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing.
 Testing report to be enclosed with the quality control documentation shipped with the boards.
17. Locations in IPC-D-356A file are given in 2.4 English units
18. South edge-to-edge connector details:
 - a. Details present in page 2 of the Molex 87783-0301 datasheet (included).

A

B

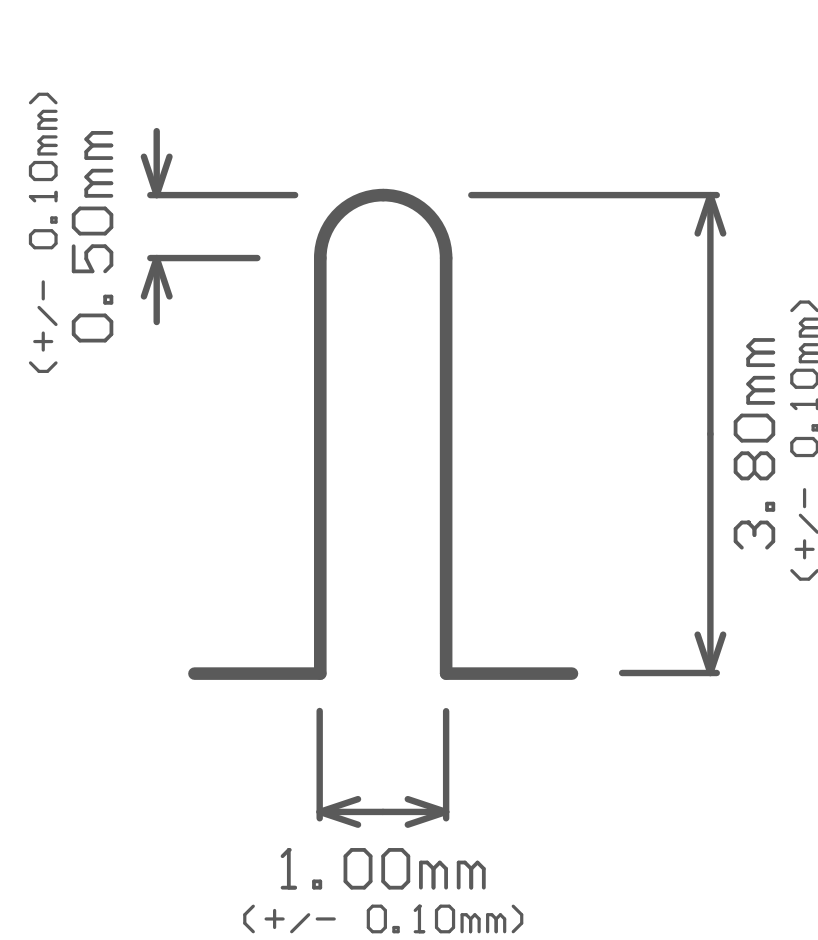
Layer Stackup



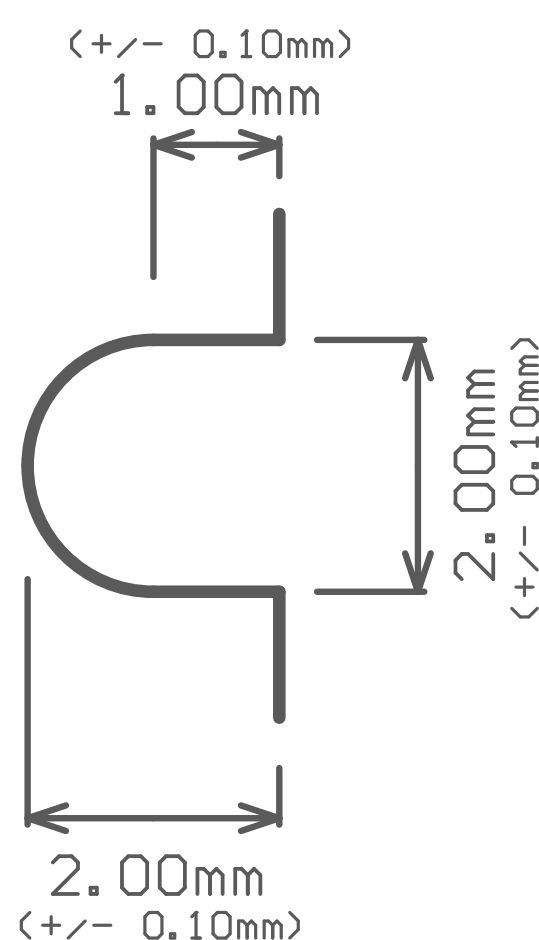
Univ. of Wisconsin—Madison Madison, WI 53706	ENGINEER: Vicente, M.	TITLE: ZYNQ—IPMC	
	PCB DESIGNER: Vicente, M.		
	DATE: 06JUN2019	PART NO.:	REV: revB1
	FILE NAME: ZYNQ_IPMC.PCBDOC	DWG NO:	SCALE: 1:1

D

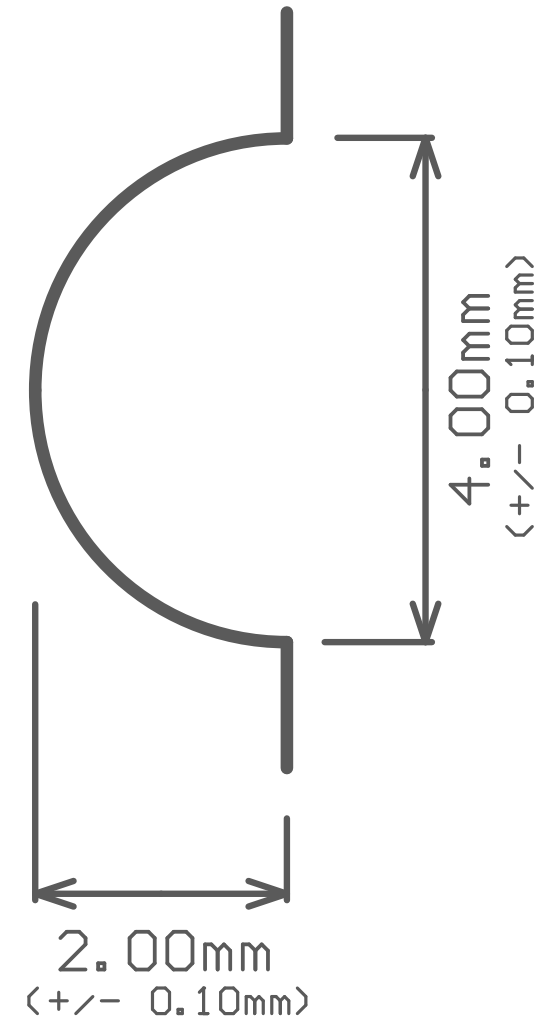
A



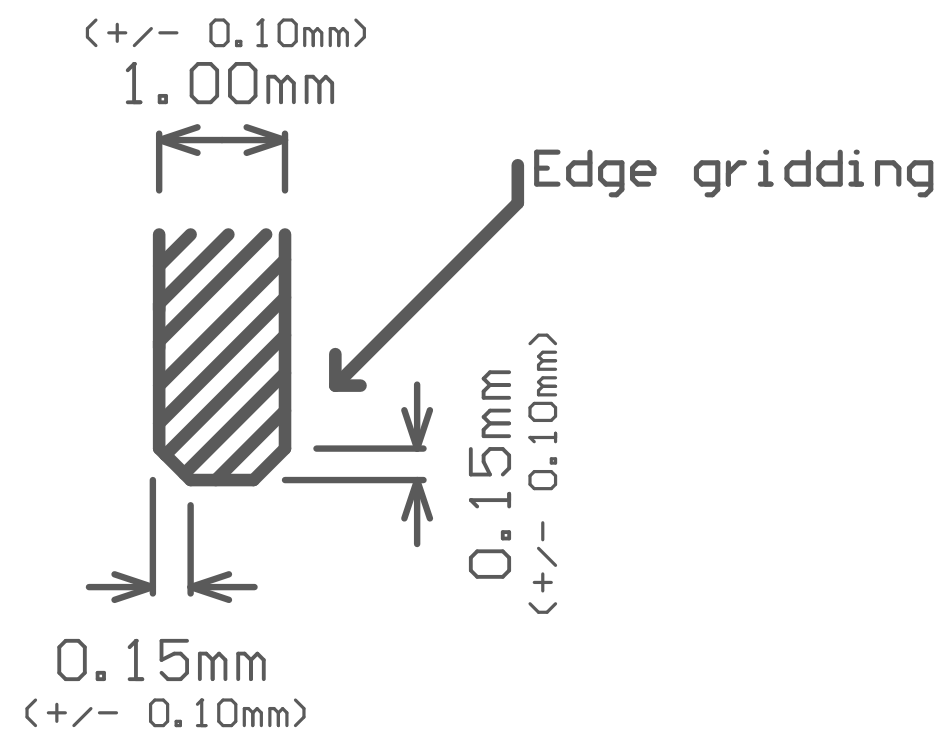
Detail 1



Detail 2



Detail 3

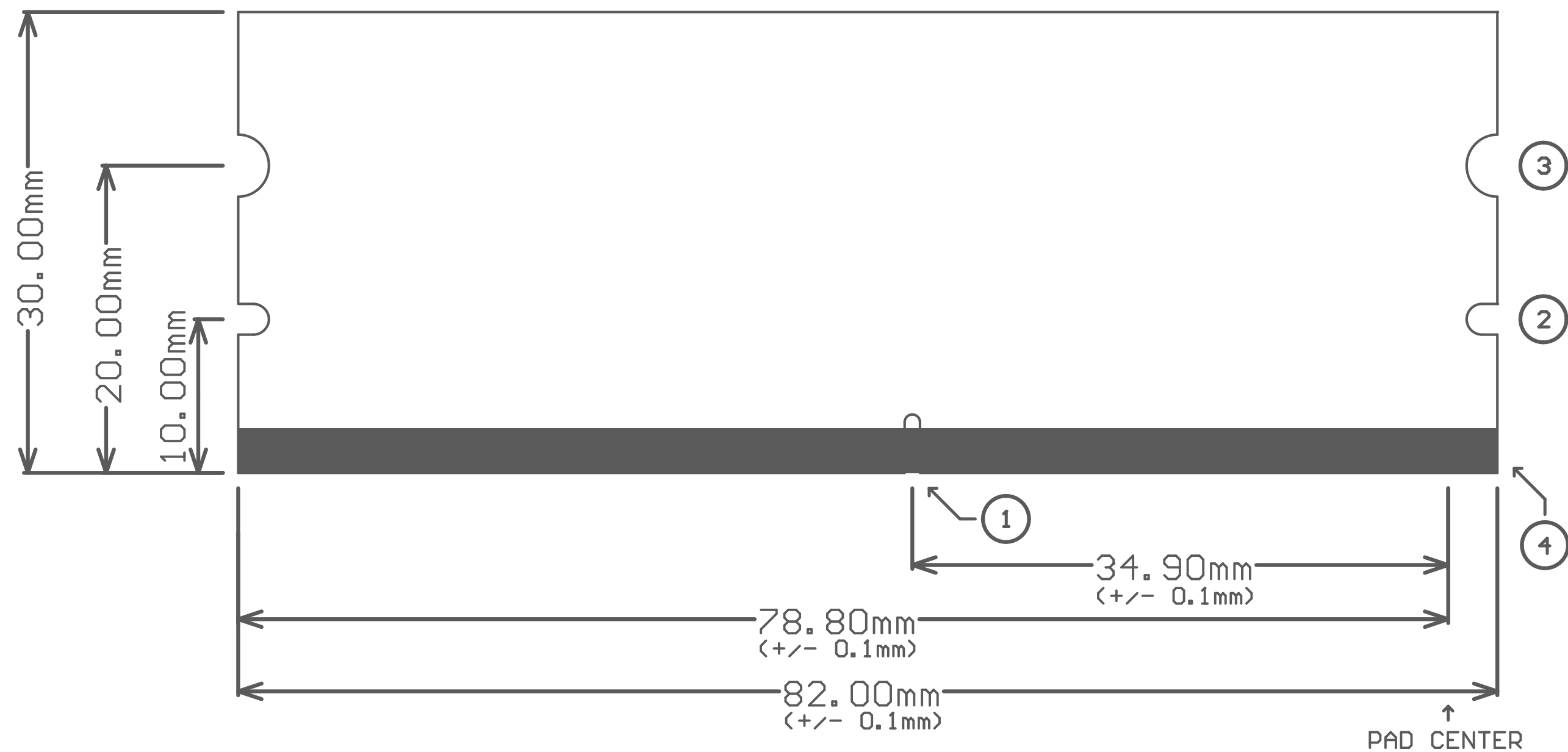


Detail 4
(PCB side view)

B

UW-IPMC MEZZANINE (revB)

Bottom Hard Gold (Mask)



C

Specifications:

- Dielectric material is Tetrafunctional FR-4 with $T_g > 170\text{ C}$
- Overall thickness is 1.0mm $\pm 0.10\text{mm}$
- Board dimensions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
- Panelization
 - Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - Panels should contain fiducial marks for X,Y alignment
- Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
- All layers use 1/2 oz. copper (before plating)
- Holes:
 - Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - Drills are plated-through holes and their locations are given in a separate drill file.
- Finish:
 - Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
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- Layers 2, 5, 6 and 9 are power planes and are INVERTED
- Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
- Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
- Combination of bow and twist shall not exceed 10 mils/inch along any direction
- Design origin is at the bottom-left corner of the PCB
- Testing:
 - All layers to undergo optical inspection (machine-based) of all layers before lamination
 - Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
- Locations in IPC-D-356A file are given in 2.4 English units
- South edge-to-edge connector details:
 - Details present in page 2 of the Molex 87783-0301 datasheet (included).

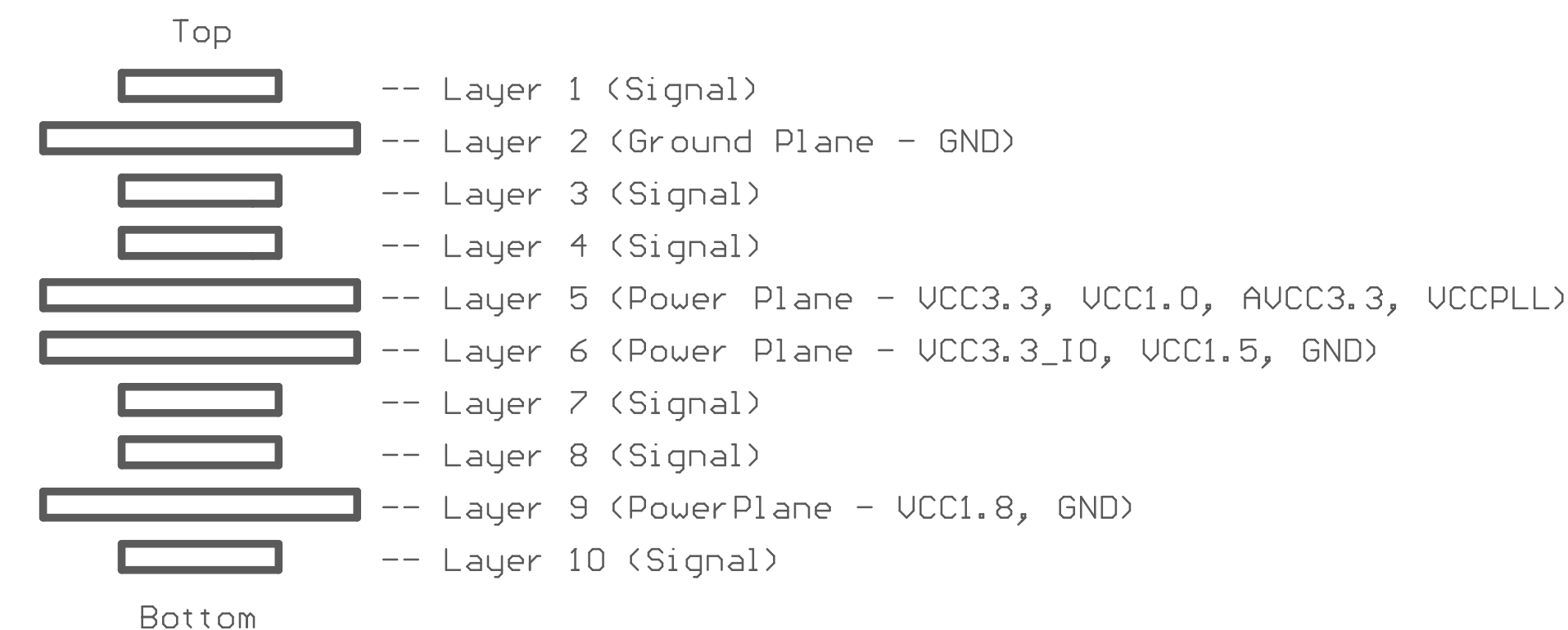
A

B

D

D

Layer Stackup



Univ. of Wisconsin—Madison Madison, WI 53706	ENGINEER: Vicente, M.	TITLE: ZYNQ—IPMC	
	PCB DESIGNER: Vicente, M.		
	DATE: 06JUN2019	PART NO.:	REV: revB1
	FILE NAME: ZYNQ_IPMC.PCBDOC	DWG NO:	SCALE: 1:1

A

B

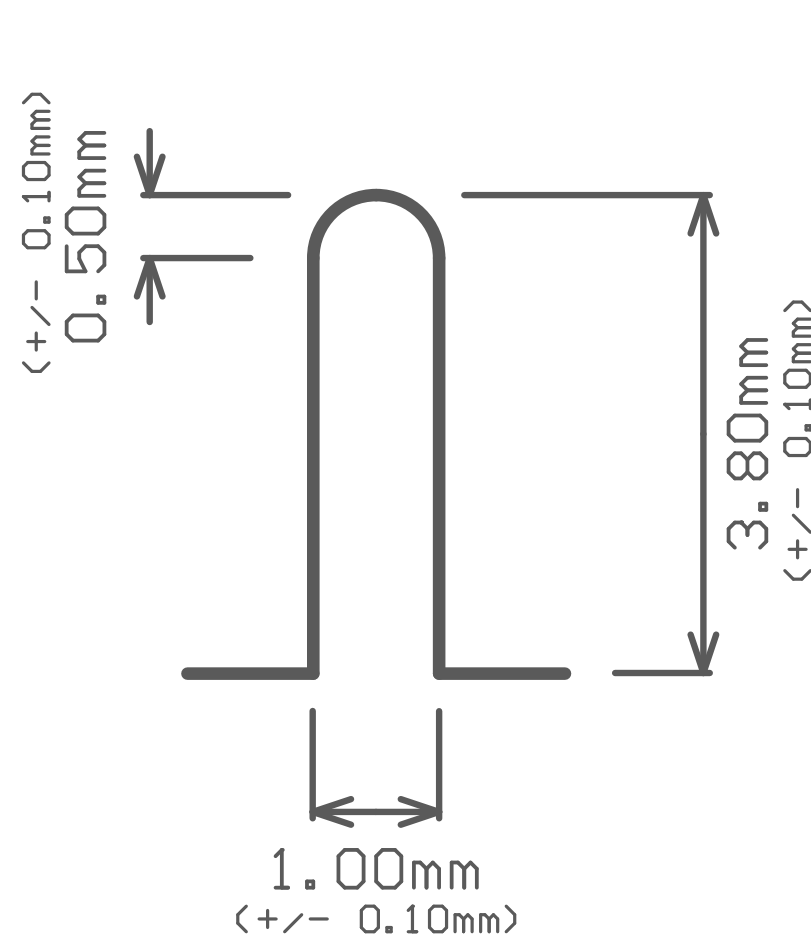
C

D

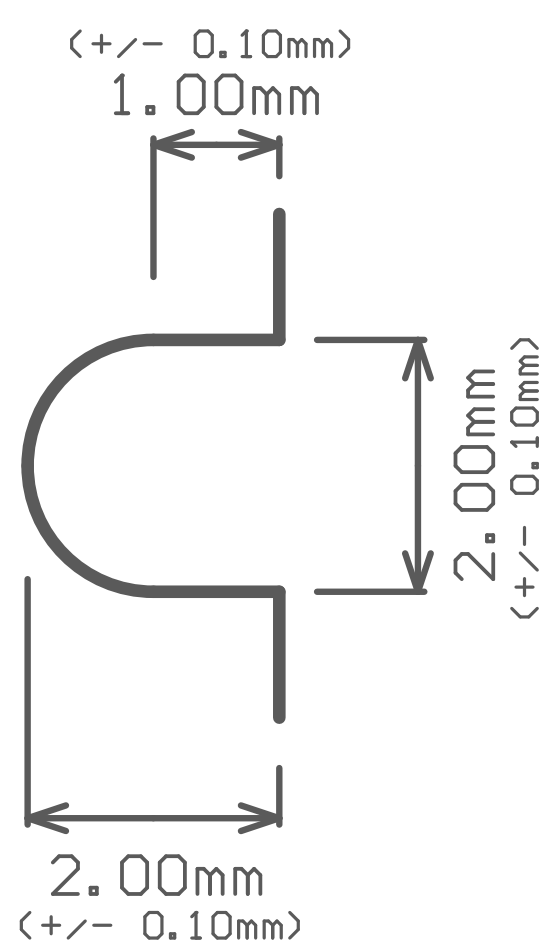
A

B

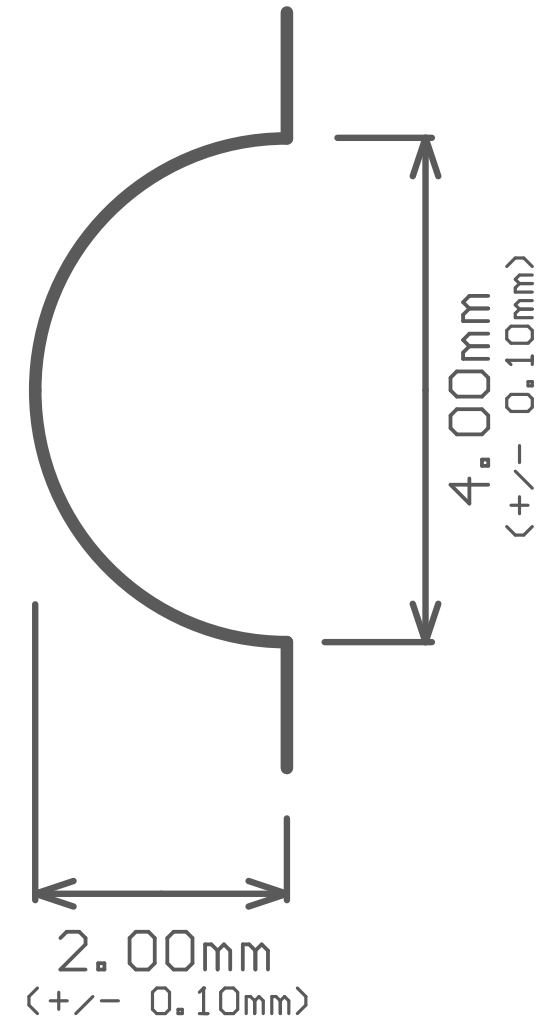
D



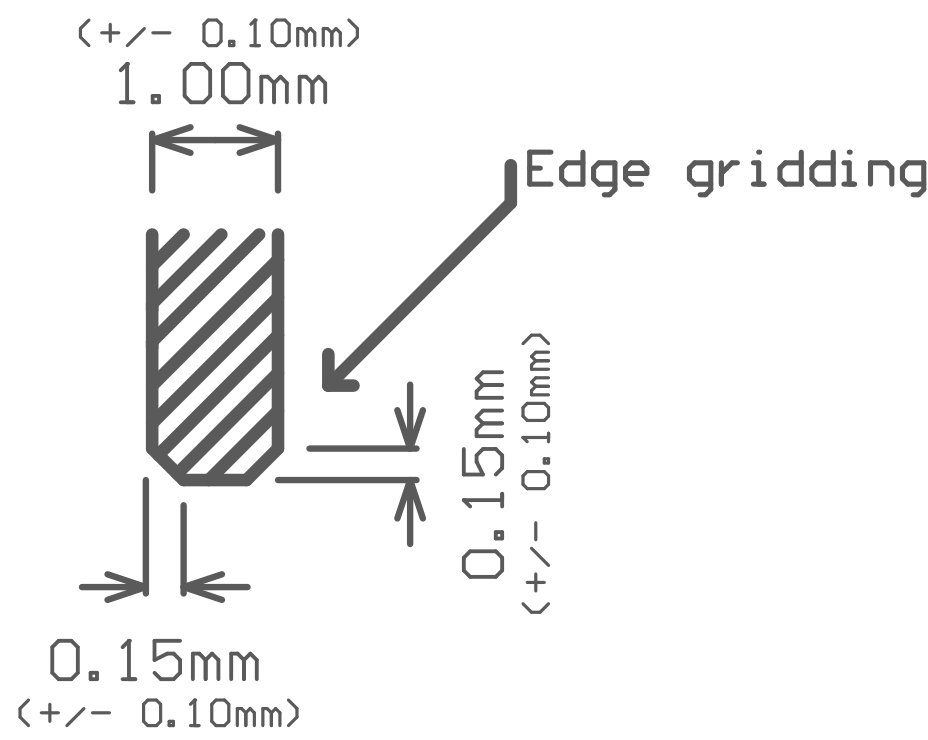
Detail 1



Detail 2

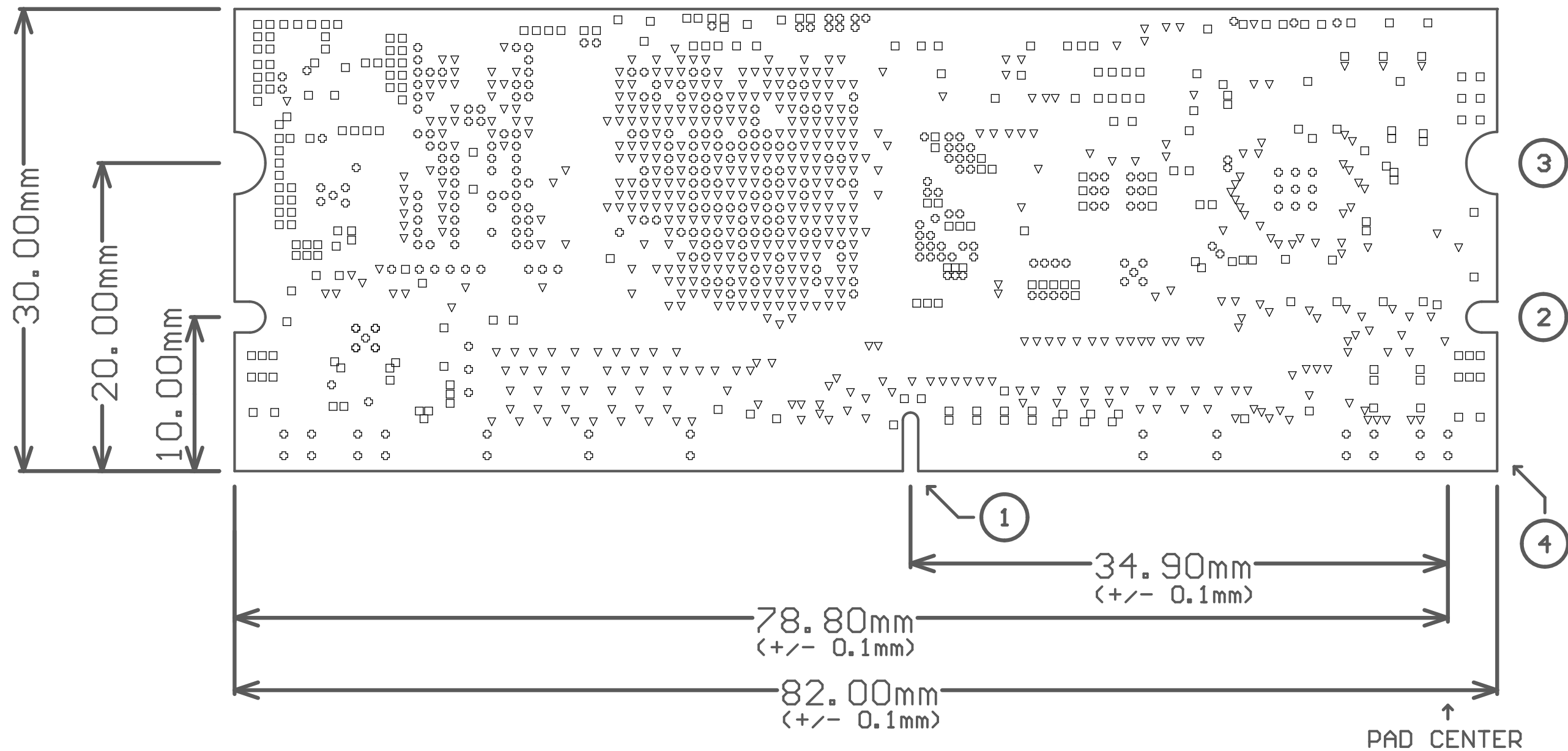


Detail 3



Detail 4
(PCB side view)

UW-IPMC MEZZANINE (revB)



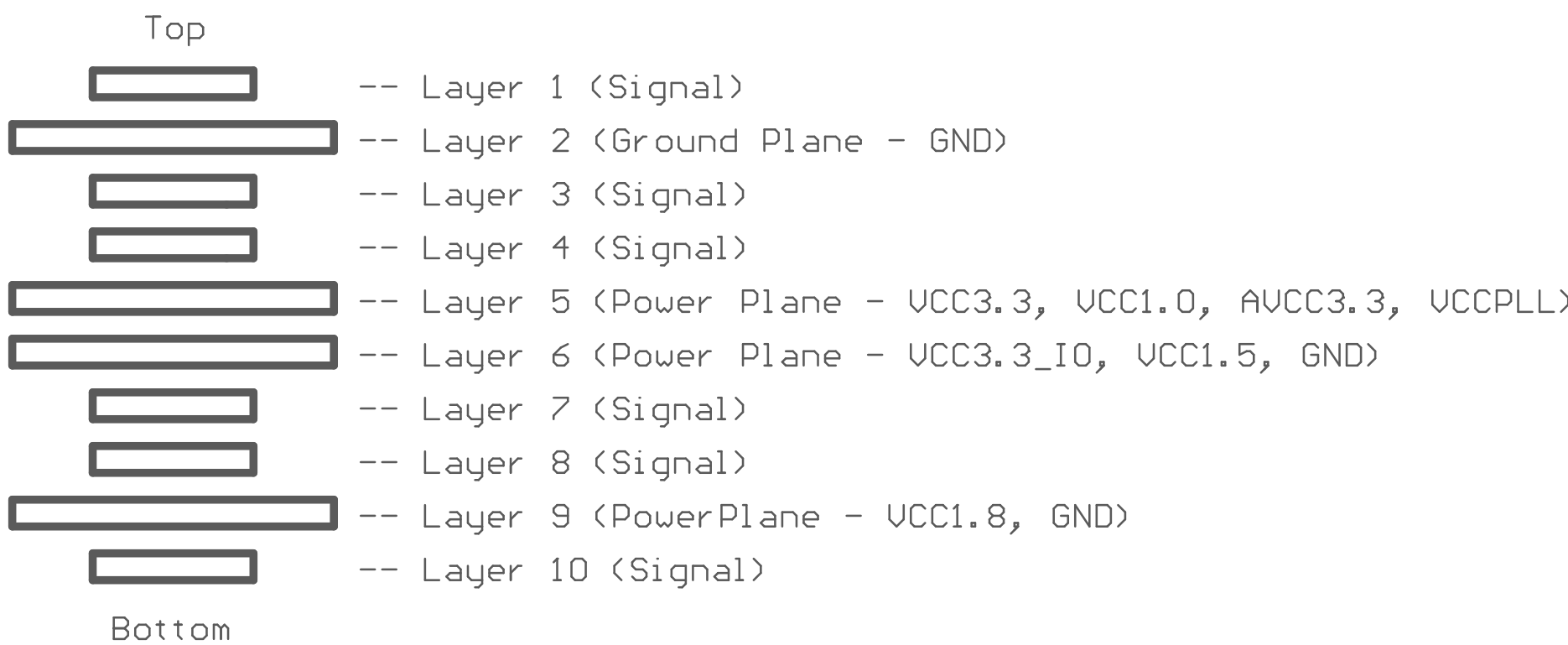
Drill Guide

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type	Physical Length	Rout Path Length
□	268	8.00mil (0.203mm)	PTH	Round	-	-
⊕	315	7.00mil (0.178mm)	PTH	Round	-	-
▽	530	6.00mil (0.152mm)	PTH	Round	-	-
	1113 Total					

Specifications:

- Dielectric material is Tetrafunctional FR-4 with $T_g > 170^\circ\text{C}$
- Overall thickness is 1.0mm $\pm 0.10\text{mm}$
- Board dimensions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
- Panelization
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- Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
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Mask shall be photoimagable, with maximum thickness of 3 mils
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- Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
- Combination of bow and twist shall not exceed 10 mils/inch along any direction
- Design origin is at the bottom-left corner of the PCB
- Testing:
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- South edge-to-edge connector details:
 - Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup



Univ. of Wisconsin—Madison
Madison, WI 53706

ENGINEER:
Vicente, M.

PCB DESIGNER:
Vicente, M.

DATE:
06JUN2019

FILE NAME:
ZYNQ_IPMC.PCBDOC

TITLE:
ZYNQ—IPMC



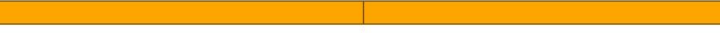







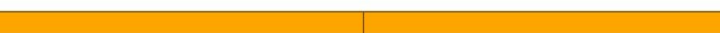





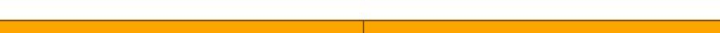



PART NO.:

REV:
revB1

DWG NO.:

SCALE:
1:1

Board Stack Report

Stack Up			Layer Stack			
Layer	Board Layer Stack	Board Layer Stack	Name	Material	Thickness	Constant
1			Top Paste			
2			Top Overlay			
3			Top Solder	Solder Resist	1.00mil	4.15
4			Component Side	Copper	2.83mil	
5			Dielectric 1		3.59mil	3.5
6			Ground Plane 1 (GND)	Copper	0.70mil	
7			Dielectric 2	FR-4	3.00mil	3.5
8			Inner Layer 1	Copper	0.70mil	
9			Dielectric 3		2.88mil	3.5
10			Inner Layer 2	Copper	0.70mil	
11			Dielectric 4		3.00mil	3.5
12			Power Plane 1	Copper	0.70mil	
13			Dielectric 5		3.58mil	3.5
14			Power Plane 2	Copper	0.70mil	
15			Dielectric 6		3.00mil	3.5
16			Inner Layer 3	Copper	0.70mil	
17			Dielectric 7		2.88mil	3.5
18			Inner Layer 4	Copper	0.70mil	
19			Dielectric 8		3.00mil	3.5
20			Power Plane 3	Copper	0.70mil	
21			Dielectric 9		3.59mil	3.5
22			Solder Side	Copper	2.83mil	
23			Bottom Solder	Solder Resist	1.00mil	4.15
24			Bottom Overlay			
25			Bottom Paste			
	Height : 41.78mil	Height : 41.78mil				

A

B

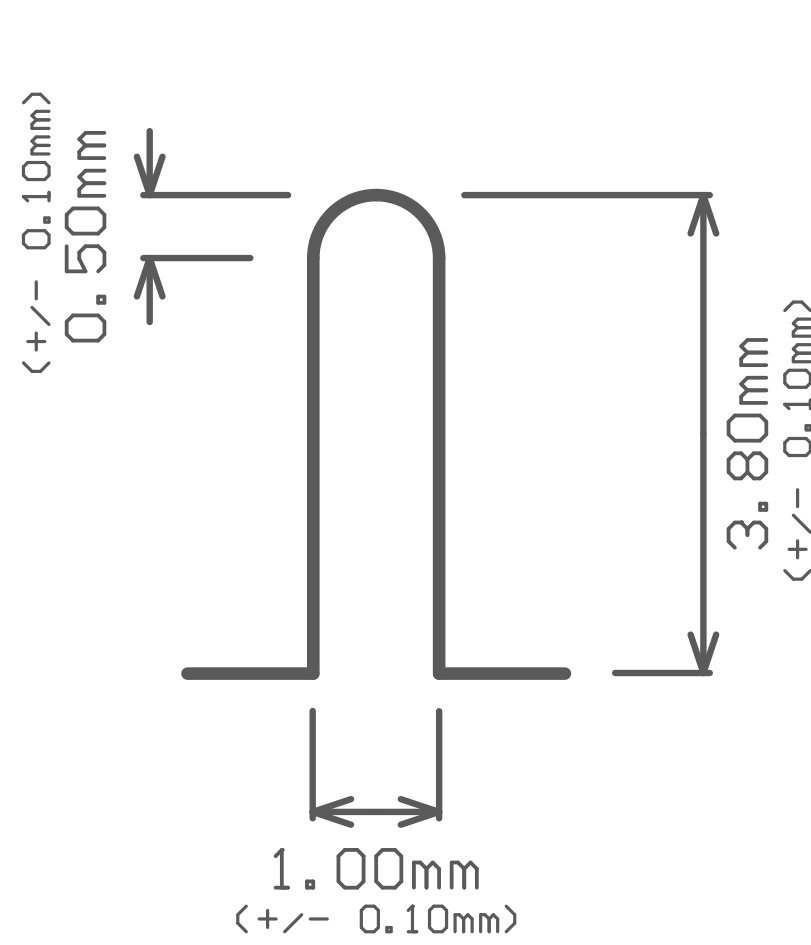
C

D

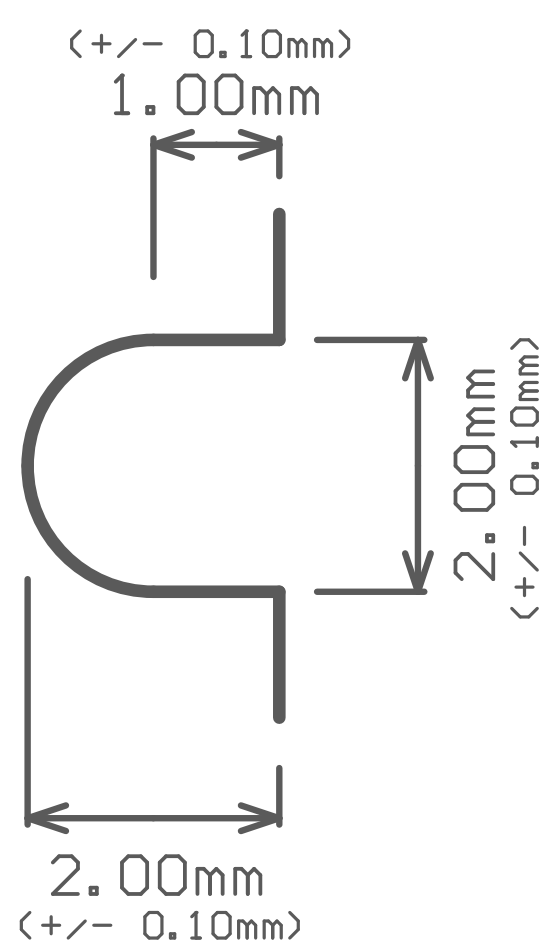
A

B

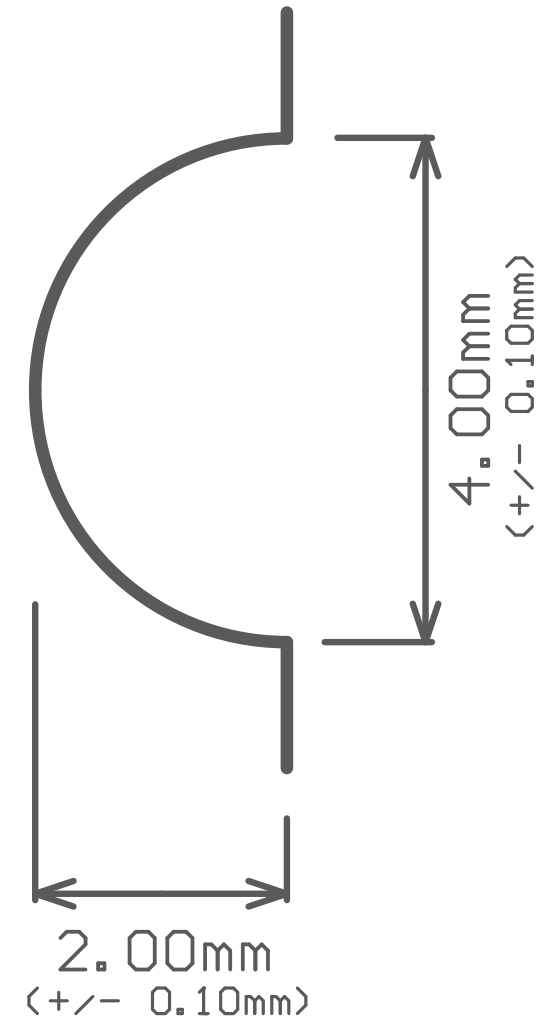
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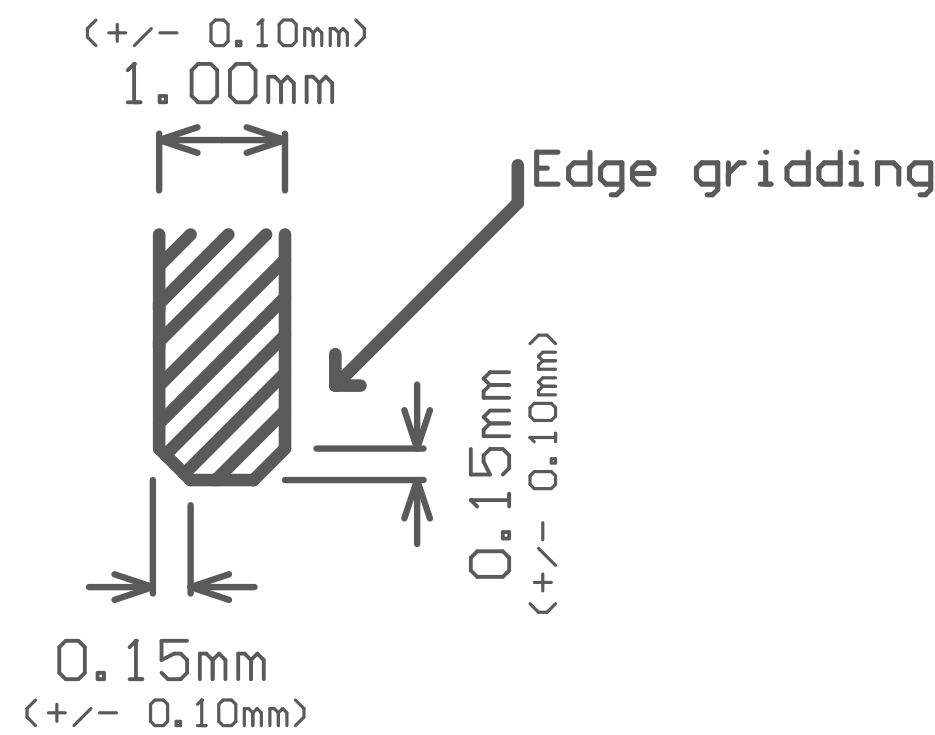
Detail 1



Detail 2

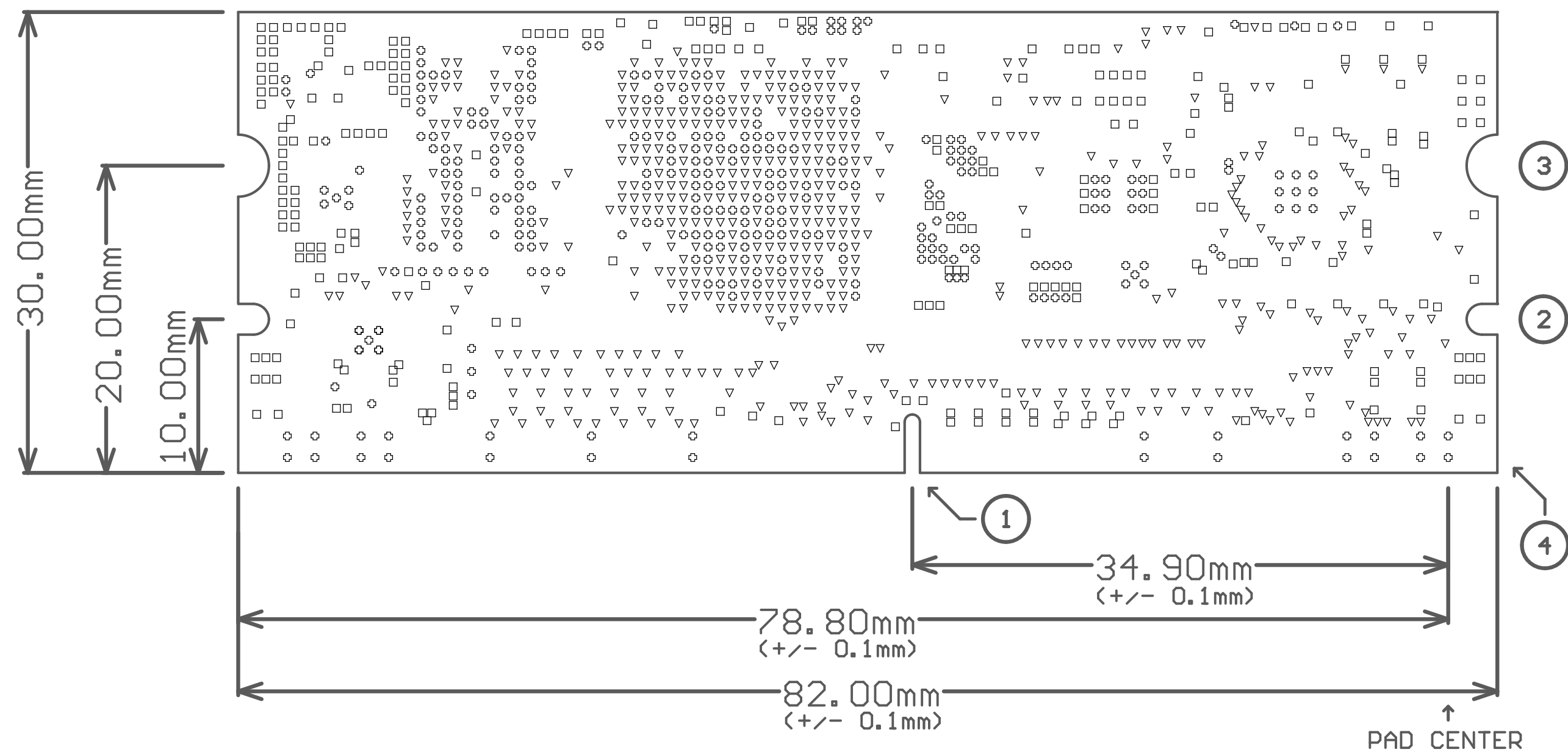


Detail 3



Detail 4
(PCB side view)

UW-IPMC MEZZANINE (revB)



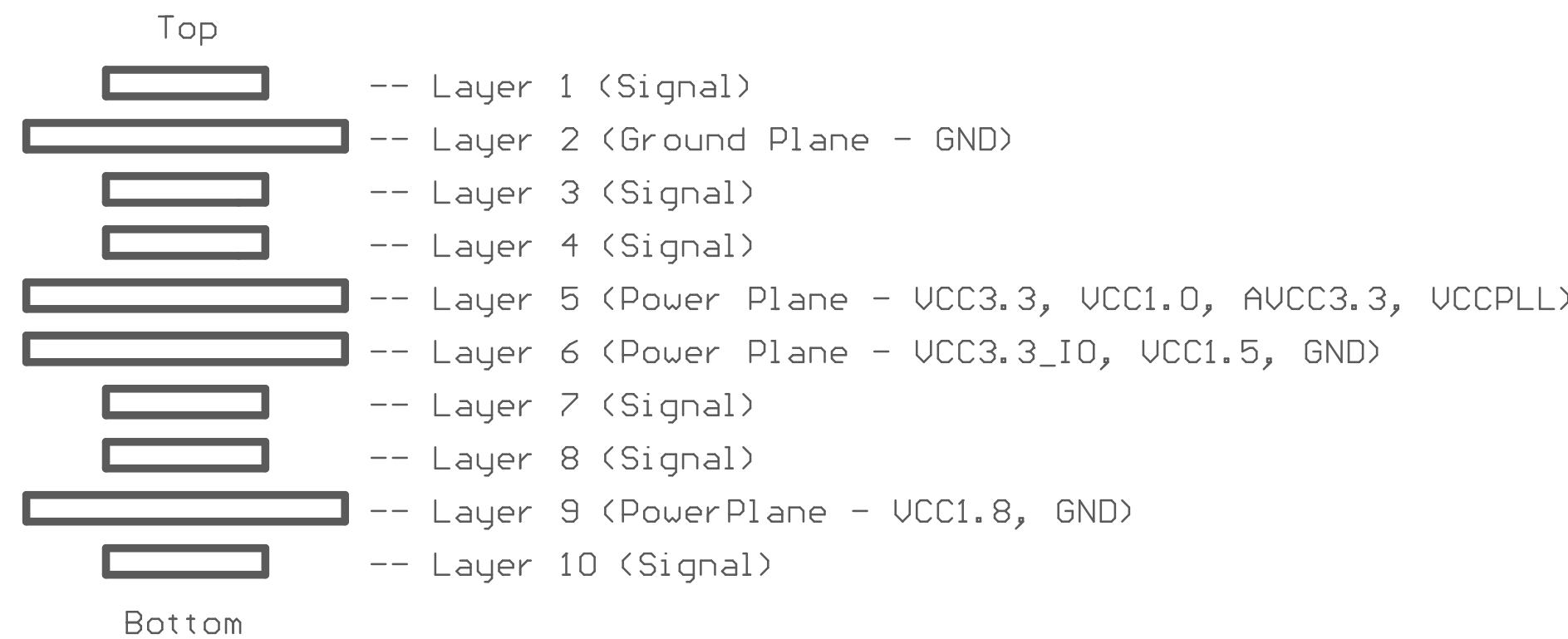
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Layer Stackup



Univ. of Wisconsin—Madison
Madison, WI 53706

ENGINEER:
Vicente, M.

PCB DESIGNER:
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